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ABSTRACT

Superconducting qubits are one of the leading approaches being investigated for building a scalable quantum computer. In the presence of external noise and perturbations plus local microscopic fluctuations and dissipation in the qubit environment, arbitrary quantum states will decohere, leading to bit-flip and phase-flip errors of the qubit. In order to build a fault-tolerant quantum computer that can preserve and process quantum information in the presence of noise and dissipation, one must implement some form of quantum error correction. Stabilizer operations are at the heart of quantum error correction and are typically implemented in software-controlled entangling gates and measurements of groups of qubits. Alternatively, qubits can be designed so that the Hamiltonian includes terms that correspond directly to a stabilizer for protecting quantum information. In this thesis, we demonstrate such a hardware implementation of stabilizers in a superconducting circuit composed of chains of π -periodic Josephson elements called a plaquette. Each plaquette consists of a superconducting loop with two conventional Josephson junctions and two inductors. We study the phase dependence of the plaquette by incorporating it into a resonant multi-loop circuit and measuring the resonator's frequency as a function of the external magnetic flux through each loop. To demonstrate the implementation of stabilizers in the Hamiltonian we made a superconducting circuit composed of a chain of three plaquettes shunted by a large capacitor. We map out the multidimensional flux space of the device by using on-chip bias lines to tune the magnetic flux through the three plaquettes independently. We measure the flux and charge dependence of the device's energy levels with microwave spectroscopy. We compare these measurements with numerical modeling of the energy level spectrum and obtain good agreement between theory and experiment for the designed and fabricated device parameters. We observe a softening of the energy band dispersion with respect to flux that is exponential in the number of frustrated plaquettes, this corresponds to the device being protected against errors caused by dephasing due to flux noise. The large shunt capacitor suppresses tunneling between the qubit logical states, and thus protects the device against bit-flip errors. A future qubit based on this design will exhibit simultaneous protection against bit-flip and phase-flip errors leading to gate errors that are significantly improved over the current state of the art.

CHARACTERIZATION OF SUPERCONDUCTING HARDWARE FOR IMPLEMENTING QUANTUM STABILIZERS

By

Kenneth Dodge

B.A., State University of New York (SUNY) Geneseo, 2014

Dissertation Submitted in Partial Fulfillment of the Requirements for the degree of Doctor of Philosophy in Physics

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Chapter 1 Introduction

Large scale quantum computers have the promise to be able to solve certain types of problems faster than is possible with traditional classical computers [1, 2]. Quantum computation relies on phenomena unique to quantum systems, such as superposition of states and entanglement. To engineer a complex quantum system that maintains its coherence long enough to do useful computations and allows for sufficiently precise control of the quantum states is immensely difficult.

The basic unit of a quantum computer is a quantum bit, or qubit. A qubit is a twostate quantum system that can be placed into an arbitrary superposition of the two states. A quantum processor needs many qubits, with the ability to control interactions between them for generating entangled states of multiple qubits. There are many different ways to physically implement a qubit, such as superconducting circuits [3], trapped ions [4], photons [5], and semiconductor quantum dots [6]. Superconducting circuits are particularly attractive because of their scalability through modern microfabrication techniques developed in the semiconductor device industry. In the presence of external noise and perturbations plus local microscopic fluctuations and dissipation in the qubit environment, arbitrary quantum states will decohere. Over the last two decades, the coherence times of superconducting qubits have improved by over five orders of magnitude [7, 8] from improvements in design, fabrication, and shielding. However, coherence times are still too short to be able to run a quantum algorithm with sufficient circuit depth to solve a useful problem faster than is possible with a classical processor. The current era of Noisy Intermediate-Scale Quantum (NISQ) technologies, which corresponds to systems with tens or hundreds of noisy qubits, still allows for the exploration of important problems, such as quantum simulation of many-body physics and quantum chemistry [9, 10, 11]. In addition, quantum supremacy, running an algorithm on a quantum processor to solve a problem, even one that has no practical application, significantly faster than is possible classically, has recently been achieved [12, 13].

In order to build a fault-tolerant quantum computer that can preserve and process quantum information in the presence of noise and dissipation, one must implement some form of quantum error correction (QEC). Much like classical error correction, quantum error correction involves building in redundancy. However, QEC is dramatically more difficult to implement compared to classical error correction because of fundamental properties of quantum mechanics, such as the no-cloning theorem and the Born measurement postulate [2]. Most approaches to QEC involve building protected logical qubits from multiple, noisy physical qubits. The surface code is one of the current leading approaches for implementing QEC [14, 15]. The quantum information represented by the logical qubit would be spread out over the many physical qubits, which allows for local errors on the physical qubits to be detected and corrected, preserving the information for longer. This is done with measurements of certain products of operators in a qubit array called stabilizers. Repeatedly measuring a quantum system using a complete set of commuting stabilizers, the system is forced into a simultaneous and unique eigenstate of all the stabilizers. Measurement of the stabilizers does not perturb the system. A change in the measurement outcome corresponds to one or more qubit errors. Encoding one logical qubit in a larger number of physical qubits, often by orders of magnitude, increases the amount of control hardware needed and makes the number of physical qubits needed to run a useful algorithm difficult to achieve. This is sometimes referred to as implementing QEC in software. Despite the challenges, initial steps towards implementing QEC with superconducting qubits have been recently achieved [16, 17].

Another approach to QEC involves desgning new types of circuits so that the protection is built into the device's Hamiltonian [18]. These new types of protected qubits promise coherence times that are not achievable with more conventional qubits. However, the implementation of protected qubit designs is at a very early stage and there are significant experimental challenges, such as requirements on parameter sizes and matching of parameter values. Most likely a combination of these hardware and

software techniques will be needed. A successful implementation of a protected qubit could lower the number of physical qubits needed to make one logical qubit.

In this thesis, I discuss our design and steps towards implementation of a protected qubit based on π -periodic Josephson elements, the charge-parity qubit. In Chapter 2, I give a brief overview of superconducting qubits, qubit decoherence, quantum error correction, and prior work on protected qubits. In Chapter 3, I give an overview of the charge-parity qubit and how it will operate. I also describe our implementation of a π -periodic Josephson element, which we call a plaquette, and the role of concatenation of plaquettes in obtaining protection. In Chapter 4, I describe the layout and fabrication of our qubit device. In Chapter 5, I describe our experiments of embedding a plaquette in an rf SQUID resonator to demonstrate its ability to act as a π -periodic Josephson element. In Chapter 6, I give a description of the experimental setup of our dilution refrigerator and measurement electronics. I also describe how we tune up the device and calibrate the multidimensional flux space. In Chapter 7, I describe our spectroscopic measurements of the device and compare them to our modeling of the device. I discuss how, although the current device is not yet effective as a qubit, it does demonstrate stabilizer terms in the device Hamiltonian. In Chapter 8, I discuss changes that could be made in future devices to make the realization of a protected charge-parity qubit possible.

Chapter 2

Background

2.1 Qubits

Just as the fundamental piece of classical information is the bit, the fundamental piece of quantum information is the qubit. Where a bit has a state of either 0 or 1, a qubit can exist in a superposition state that is a linear combination of $|0\rangle$ and $|1\rangle$:

$$|\psi\rangle = \cos(\theta/2)|0\rangle + \sin(\theta/2)e^{i\phi}|1\rangle, \qquad (2.1)$$

where $|0\rangle$ and $|1\rangle$ are the qubit basis states. θ and ϕ can be visualized as polar and azimuthal angles on the Bloch sphere representation of the qubit state, where the north pole is $|0\rangle$ and the south pole is $|1\rangle$. We need to preserve the polar and azimuthal angles to preserve the information in the qubit, which is necessary for successfully running an algorithm on a quantum computer. While a classical bit can only experience one type of error, when a 0 flips to a 1 and vice versa, a qubit is subject to both bit-flip and phase-flip errors. These errors are characterized by two different errors in the amplitude and phase that are known as bit-flip and phase-flip errors, respectively; these are characterized by two different timescales, the depolarization or relaxation time, T_1 , and the pure dephasing time, T_{ϕ} , respectively. Phase-flip errors are associated with low-frequency noise that modulates the qubit frequency and causes superpositions to dephase. Bit-flip errors are associated with noise at the qubit frequency that drives transitions between the qubit basis states. Both of these types of errors lead to decoherence of the qubit state.

2.2 Josephson junctions



Figure 2.1: a) Diagram of a SIS (superconductor-insulator-superconductor) Josephson junction. b) The electrical symbol of a Josephson junction. c) A scanning electron micrograph of an Al-AlO_x-Al junction that was fabricated in our lab.

Superconducting circuits are a promising medium for making qubits due to the low loss, macroscopic phase coherence, and ability to be made with traditional semiconductor fabrication techniques. One of the main building blocks used to make nearly all superconducting circuits is the Josephson junction.

A Josephson junction is made from two superconducting electrodes separated by a thin insulating barrier with a typical thickness of the order of 1 nm. The dynamics of a Josephson junction are described by the Josephson relations [19, 20]:

$$I(t) = I_0 \sin \varphi(t), \qquad (2.2)$$

$$V(t) = \frac{\Phi_0}{2\pi} \frac{\partial \varphi(t)}{\partial t},$$
(2.3)

where φ is the phase difference of the wavefunctions for the Cooper pairs in the electrodes on either side of the junction, V is the voltage across the junction, I is the current through the junction, I_0 is the maximum supercurrent that the junction can support, and $\Phi_0 \equiv h/2e$ is the magnetic flux quantum. These two relations can be used to derive the Josephson inductance

$$L_J = \frac{\Phi_0}{2\pi I_0 \cos \varphi(t)},\tag{2.4}$$

$$L_J = \frac{\Phi_0}{2\pi I_0 \sqrt{1 - I^2 / I_0^2}}.$$
(2.5)

The inherent nonlinearity of this inductance is what makes it so useful as a circuit element. Using chains of junctions, it is possible to implement a large compact inductance [21, 22]. The Josephson energy can also be derived

$$E_{J0} = \frac{\Phi_0 I_0}{2\pi},$$
 (2.6)

$$E_J = E_{J0} \cos \varphi, \tag{2.7}$$

which has a 2π -periodic dependence on phase.

2.3 Conventional Superconducting Qubits

At present, most state-of-the-art superconducting qubits are made by creating a weakly anharmonic oscillator, where Josephson junctions provide the nonlinearity needed to make the circuit anharmonic, and using the two lowest levels as the two states of the qubit.

One of the early examples of a superconducting qubit was the Cooper pair box [23], which consists of a small superconducting island with small capacitance to ground that is connected to ground through a Josephson junction. Cooper pairs can tunnel on/off the island depending on the offset charge bias coupled to the island through a gate capacitance. Dephasing times for this qubit were short because the qubit frequency depended strongly on the offset charge on the island, which fluctuated significantly due to the dynamics of microscopic defects in the qubit environment. The successor to this qubit was the transmon (Fig. 2.2). The transmon operates in a different regime by increasing the capacitance shunting the junction [24]. This increased capacitance flattens the qubit's response to the offset charge on the island making it insensitive to charge noise [25]. Thus, the first transmons exhibited dramatically



Figure 2.2: a) Schematic of a transmon. E_J is the Josephson energy of the junction and $E_C = e^2/2C$ is the charging energy of the shunt capacitor. Large E_J/E_C results in decreased charge dispersion and insensitivity to charge noise. b) The cosine potential of the transmon results in an anharmonic oscillator. The lowest two levels are used as the computational states.

improved dephasing times compared to the earlier Cooper pair box qubits [26, 27]. Improvements in fabrication [28, 29, 30] and filtering [31, 32] have reduced the number of loss channels coupled to the qubit and the environmental noise at the qubit frequency. Current state-of-the-art transmons have T_1 times of the order of hundreds of microseconds [33].



Figure 2.3: a) Schematic of a fluxonium qubit. E_J is the Josephson energy of the junction, E_C is the charging energy, and E_L is the inductive energy. b) The potential of the fluxonium qubit at frustration with nearly degenerate ground and first excited state.

To further improve depolarization times, one can build a qubit that has disjoint wavefunctions for the two qubit states. This leads to smaller qubit transition matrix elements and reduces the qubit's susceptibility to noise at the qubit frequency and greatly reduces the rate of bit-flip errors. One example of this approach is the heavy fluxonium qubit. A heavy fluxonium qubit consists of a small Josephson junction shunted with a large capacitor and a large inductor (Fig. 2.3a) [34, 22]. The two qubit states correspond to the lowest two degenerate wells in the potential energy landscape that are separated by a large barrier when the qubit is frustrated by an external magnetic flux (Fig. 2.3b). T_1 times of order 1 ms have been realized with this approach [35, 36]. However, the protection against bit-flips comes with a trade off. These qubit levels disperse with flux, so flux noise will limit the dephasing time, although, the splitting of the ground-state doublet at frustration due to tunneling between the wells provides a modest level of protection against flux noise over a narrow range of flux.

2.4 Quantum Error Correction

Protecting fragile information in quantum processors from decoherence requires some form of quantum error correction (QEC). With typical QEC techniques, for example, Kitaev's toric code [37] and the surface code [14], stabilizing a single logical qubit requires a large number of physical qubits. This traditional approach to QEC can be considered as implementing QEC in software. Performing repeated stabilizer operations, consisting of entangling gates and measurements of tensor products of operators on multiple qubits in the array, protects the logical qubit against bit-flip and phase-flip errors.

Two examples of stabilizers for a pair of qubits A and B are XX and ZZ, which are the same as the tensor products of Pauli operators $\hat{\sigma}_{xA} \otimes \hat{\sigma}_{xB}$ and $\hat{\sigma}_{zA} \otimes \hat{\sigma}_{zB}$. XXand ZZ commute, so measurements of these two operators are compatible and the two-qubit state can be a simultaneous eigenstate of both [14]. The four eigenstates of these stabilizers are the Bell states. If we measure these two stabilizers, the eigenvalues we obtain will determine which of the Bell states the qubits are in, although we obtain no information about the state of either qubit individually. If there are no external errors, then repeated measurements of XX and ZZ will always reveal the same state.

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If there is a bit-flip or phase-flip error on one of the qubits, corresponding to an X or Z operation on the qubit, then the subsequent measurement of the XX and ZZ stabilizers will yield a different result and we will know an error occurred, after which the error can be corrected by applying an appropriate qubit gate depending on the results of the stabilizer measurements.

The overhead requirements for QEC, e.g., the number of physical qubits required to form one protected logical qubit, depends on the error rates of the physical qubits. There is a certain error threshold rate, that depends on the particular code, to break even with QEC. If the error rate is above this threshold, then running QEC will actually make things worse and the lifetime of the quantum information will decrease. If the physical qubit error rate is below this threshold, QEC will improve the lifetime of the quantum information [38]. For the surface code, this error threshold is roughly 1% per operation [14]. However, for physical qubit error rates just below the threshold, one requires thousands of physical qubits to implement a single logical qubit with sufficiently low logical error rate for achieving fault tolerance. Thus, implementing QEC is extremely challenging, but initial steps have been made to demonstrate an improvement in quantum information lifetime [39, 15, 40, 17, 16].

2.5 Protected Qubits

As an alternative, designing systems that implement stabilizers directly in hardware would protect against decoherence from local noise while reducing the requirements for repeated entangling gates and measurements that are necessary for running QEC in software. Such an approach could be a key enabling step for fault-tolerant quantum processors, with lower overhead requirements on the physical qubit array size and control complexity. The goal is to develop a qubit that is exponentially protected against both bit-flip and phase-flip errors. Exponential protection means that there is some device parameter that can be adjusted to cause improvements in the error rate that are exponential in that parameter.

A variety of superconducting qubit designs with intrinsic protection against decoherence have been studied previously, including rhombi arrays [41, 42, 43], the $0-\pi$ qubit [44, 45, 46], the two-Cooper-pair tunneling qubit [47], and bifluxon qubit [48]; summaries of these approaches may also be found in the review articles of Refs. [18, 49]. Many of these protected qubit designs rely on excessively large inductances at high frequencies, which are hard to achieve because the size leads to unwanted parasitic capacitances. The $0-\pi$ and two-Cooper-pair tunneling qubits have stringent demands on matching of circuit parameters, such as Josephson junctions and inductances, which makes fabrication difficult. In this thesis, we demonstrate the implementation of quantum stabilizers in superconducting hardware with a circuit design referred to as the charge-parity qubit. Through local flux control of the circuit elements, we observe signatures of stabilizer terms in the device Hamiltonian with spectroscopic measurements of exponential flattening of the energy bands with respect to flux, as well as characteristic periodic modulation with offset charge on various superconducting islands as we tune the device between regimes with different levels of protection.

Chapter 3

Introduction to the charge-parity qubit

In this chapter, I describe the basics of the charge-parity protected qubit design and the implementation of a π -periodic element using dc SQUIDs.

3.1 Plaquette Qubit

Similar to previous protected qubit designs, our device is based on π -periodic Josephson elements [50, 51], where the Josephson energy varies like $\cos 2\varphi$, where φ is the difference in the superconducting phase across the Josephson element. In this case, charge transport consists of the coherent tunneling of 4e, or pairs of Cooper pairs, rather than 2e in the case of a conventional Josephson junction. We implement each of these elements with a plaquette formed from a dc Superconducting QUantum Interference Device (SQUID), consisting of two conventional Josephson junctions and a non-negligible loop inductance. When flux biased at $\Phi_0/2$, where $\Phi_0 \equiv h/2e$, the first order term in the Josephson energy that is proportional to $\cos \varphi$ vanishes. This leaves a second order Josephson energy term $E_2 \cos 2\varphi$, with sequential minima separated by π , where the energy scale E_2 depends on the Josephson energies of the individual Josephson junctions E_J and the inductive energy of the SQUID loop inductance E_L . The phase φ is therefore a compact variable residing on a circle. With the flux bias moved below (above) frustration ($\Phi_0/2$), the π wells are raised above (below) the 0 wells [Fig. 3.1b,c]; at a flux bias of 0 mod Φ_0 , the potential becomes $\propto \cos \varphi$, as in a conventional Josephson junction. The connection between plaquettes and dc SQUIDs is discussed in more detail in Sec. 3.2.

For a single plaquette biased at $\Phi_0/2$ with a large capacitive shunt C_{sh} [Fig. 3.1a], tunneling between the $0/\pi$ wells will be suppressed. The wavefunctions in the $0/\pi$ wells are thus disjoint and the device is protected against bit-flip errors in the phase basis. At the same time, the circuit wavefunctions will be spread out in the charge basis, corresponding to superpositions of even (odd) multiples of Cooper pairs on the logical island where the plaquette is connected to C_{sh} for the 0 (π) states in the phase basis. This protects the qubit against dephasing from charge noise, similar to a transmon. As the flux is tuned away from frustration, the energy levels disperse linearly [Fig. 3.1d], thus exhibiting no protection against phase flips due to flux noise.

We expect to see a phenomenon analogous to the Aharonov-Casher effect when the offset charge on the shunt capacitor is tuned. The Aharonov-Casher effect is the dual of the Aharonov-Bohm effect. It describes how when a magnetic flux is moved around a charge, it acquires a phase that is dependent on the path that it took [52, 53]. In the case of the plaquette, the Aharonov-Casher effect is in the abstract phase space describing the plaquette dynamics. Since the phase across the plaquette is a compact variable, it can travel from the 0 well on one side of the circle to the π well on the other side of the circle either by going clockwise or counterclockwise. These two paths will acquire a different phase depending on the offset charge on the C_{sh} logical island. This will cause the splitting between levels in the 0 and pi wells to modulate with offset charge. The splittings for the ground and first few excited states are small, but nonzero, so they are difficult to observe. But splittings due to tunneling between higher levels near the top of barrier are larger, and thus easier to see the charge modulation. Asymmetries between the junctions in the plaquette will reduce the interference and depth of modulation of the various gaps with offset charge.

We next consider concatenation of multiple plaquettes in series while maintaining the large shunt C_{sh} across the 1D array. At double frustration, when two adjacent plaquettes are simultaneously frustrated, there are four minima in the two-dimensional surface defined by the common-mode phase variables for each of the two plaquettes: $00, \pi\pi, 0\pi, \pi0$ [Fig. 3.1f]. This surface has the topology of a torus, since φ for each plaquette is a compact variable with 2π periodicity. If the capacitance to ground of the intermediate island between the plaquettes, C_{isl} , is sufficiently small, with a



Figure 3.1: (a) Schematic of single π -periodic plaquette shunted by capacitance C_{sh} , (b) cos 2φ potential at frustration ($\Delta \Phi = \Phi - \Phi_0/2 = 0$) with localized wavefunctions in 0 and π wells. (c) Potential for $\Delta \Phi < 0$, raises π wells above 0 wells, (d) Linear dispersion of 0 and π levels with respect to $\Delta \Phi$ for vanishing tunnel splitting. (e) Schematic of two series π -periodic plaquettes shunted by capacitance C_{sh} with small capacitance C_{isl} from intermediate island to ground, (f) Contour plot of potential with respect to phase across each plaquette; periodic boundary conditions correspond to topology of a torus. (g) 1D cuts of potential between 00 and $\pi\pi$ wells along $\phi_1 = \phi_2$ (left) and 0π and $\pi 0$ wells along $\phi_1 = \phi_2 + \pi$ (right) at double frustration ($\Delta \Phi_1 = \Delta \Phi_2 = 0$) with hybridized wavefunctions for symmetric (blue) and antisymmetric (red) superpositions, (h) 1D cut of effective potential along $\phi_1 = -\phi_2$ at double frustration, (i) Quadratic dispersion of even-parity (odd-parity) levels and flat dispersion of odd-parity (even-parity) levels near double frustration for simultaneous scan of plaquette fluxes along $\Delta \Phi_1 = \Delta \Phi_2$ ($\Delta \Phi_1 = -\Delta \Phi_2$) on left (right) plot.

charging energy $E_C^{isl} = (2e)^2/2C_{isl} \sim E_J$, quantum fluctuations of the island phase lead to hybridization along the direction between wells of the same parity, so, $00/\pi\pi$ and $0\pi/\pi 0$. In this case, the levels with the same parity of the plaquettes develop a splitting near double frustration, with the ground states corresponding to symmetric superpositions: $00 + \pi\pi$ for even parity, and $0\pi + \pi 0$ for odd parity. There are then excited states given by the antisymmetric superpositions: $00 - \pi\pi (0\pi - \pi 0)$ for even (odd) parity. The gap between the symmetric and antisymmetric states is Δ_{SA} . The two hybridized ground states of opposite parity then form the logical states for the device: $00 + \pi\pi$ and $0\pi + \pi 0$ [Fig. 3.1h]. Larger E_C^{isl} results in a larger gap between the symmetric states of the same parity and flatter bands at double frustration [Fig. 3.1i]. The splitting and flattening thus corresponds to an XXstabilizer term of the two plaquettes in the Hamiltonian,

$$H_{stab} \propto \Delta_{SA}(X \otimes X), \tag{3.1}$$

and the resulting flattening provides protection against dephasing due to flux noise. This softening of the flux dispersion at frustration is exponential in the number of plaquettes in the chain, thus, quadratic dispersion for two plaquettes, cubic for three plaquettes, and so on. At the same time, the large C_{sh} still suppresses tunneling between the logical states of opposite parity, thus preserving exponential protection against bit-flip errors.

Similar to the tuning of the energy gaps between 0 and π well states with offset charge on the C_{sh} island at single frustration, there will be Aharonov-Casher interference of tunneling paths in phase space that lead to the charge modulation of Δ_{SA} at double frustration by tuning the offset charge to the intermediate island.

In order to implement plaquette chains that exhibit clear stabilizer behavior, we target a three-plaquette device with $E_J \sim E_L \sim 1.5 \,\mathrm{K}$ ($k_B = 1$), where E_L is the inductive energy $(\Phi_0/2\pi)^2/L$ of the inductance L on each arm of a plaquette. If the ratio of E_J/E_L is too small, E_2 vanishes. If E_J/E_L is too large, the energy levels depend so strongly on flux that even if there are large quantum fluctuations, we lose protection from flux noise. Additionally, we target the charging energy of each junction in the plaquette $E_C = (2e)^2/2C_j \sim 4 \,\mathrm{K}$, where C_j is the junction capacitance. This refers to the energy of a Cooper pair so there is a factor of 4



Figure 3.2: (a) Schematic for single π -periodic plaquette. (b) Potential energy vs. phase across $\cos 2\varphi$ element for frustration (top), and 40 m Φ_0 away (bottom); lines indicate example plasmon (red) and heavy fluxon (blue) transitions. (c) Schematic for concatenated π -periodic plaquettes. (d) Sketch of contour plot of effective potential at double frustration accounting for different effective masses plotted as a function of the phase across each plaquette with periodic boundary conditions; lines indicate plasmon (red), plus heavy (blue) and light (magnenta) fluxon transitions. Level diagrams around frustration for (e) single plaquette, (f) two concatenated plaquettes.

difference compared to the definition of E_C in Fig. 2.2 where it referred to the energy of a single electron. These E_J and E_C values can be achieved with conventional small-area Al-AlO_x-Al Josephson junctions, although with significantly larger critical current densities than would be used in a typical transmon qubit. We implement inductors in each plaquette with chains of large-area Josephson junctions, similar to typical fluxonium designs [54]. We have also explored the use of nanowires patterned from high kinetic inductance superconducting films for the plaquette inductors [55].

In order to demonstrate the implementation of stabilizers, we will compare the flux dispersion of the energy bands for different frustration conditions of the various plaquettes. When only one of the plaquettes in the chain is near frustration, we expect to see linear dispersion with flux. When two of the plaquettes are brought near frustration we expect to see quadratic dispersion with flux that corresponds to protection against flux noise. When all three of the plaquettes are near frustration we expect to see flatter cubic dispersion with more protection from flux noise. Before examining experimental spectroscopy scans, we consider the expected level structure and define the various types of transitions. In Fig. 3.2 we plot numerically modeled energy-level diagrams for our experimental device parameters at single frustration, where one plaquette is biased at $\Phi_0/2$ and the other two are at Φ_0 , and double frustration, where Plaquettes 1 and 2 are biased at $\Phi_0/2$ and Plaquette 3 is biased at Φ_0 . The modeling of the plaquette energy levels are described more in Chapter Following convention, we refer to transitions between levels in the same well, 7. which disperse with the same sign with respect to flux, as *plasmons*; transitions between wells with opposite parity on the logical island that disperse with flux with the opposite sign are *heavy fluxons* because of the vanishingly small gap for low-lying level crossings due to the large effective mass from C_{sh} . Transitions between levels of the same parity but opposite symmetry, for example, $00 + \pi\pi$ to $00 - \pi\pi$, disperse sharply with flux; we thus refer to these transitions as *light fluxons* due to the low effective mass in this direction from the small C_{isl} .

3.2 π -periodic element

Here I examine the behavior of an individual π -periodic plaquette in more detail (Fig. 3.3). Each junction of the plaquette has a critical current I_0 and $E_J = \Phi_0 I_0/2\pi$;



Figure 3.3: (a) Circuit schematic for dc SQUID plaquette. 2D potential as a function of common-mode (δ_p) and differential (δ_m) phase variables at external flux bias Φ_{ex} of (b) 0, (c) $\Phi_0/2$. (d) Linecut along δ_m for $\delta_p = 0$ for $\Phi_{ex} = 0$. (e) Linecut between adjacent minima vs. δ_m for $\Phi_{ex} = \Phi_0/2$. (f) Linecut along δ_p at $\delta_m = 0$ for $\Phi_{ex} = 0$. (g) Linecut between adjacent minima vs. δ_p for $\Phi_{ex} = \Phi_0/2$.

the inductance in each arm of the SQUID L is related to the inductive energy $E_L = (\Phi_0/2\pi)^2/L$. In order to understand the origin of the $\cos 2\varphi$ potential, we consider the two-dimensional potential energy landscape as a function of the two junction phases, δ_1 and δ_2 , which is determined by E_J , E_L , and the external flux bias Φ_{ex} [56]. For now, we consider symmetric plaquettes where both junction critical currents are identical; later in this section we will consider the effects of junction asymmetry. Following convention for dc SQUIDs we plot the potential energy in terms of the common-mode and differential phase variables: $\delta_p = (\delta_1 + \delta_2)/2$ and $\delta_m = (\delta_2 - \delta_1)/2$. The phase dependence of the Josephson energy for each junction results in a 2D washboard pattern of potential minima. At the same time the inductive energy associated with circulating currents flowing through the inductors corresponds to a parabolic sheet with its minimum along a line running parallel to δ_p . Changing Φ_{ex} shifts where the minimum of this inductive parabolic sheet falls with respect to the minima in the potential.

For a flux bias at unfrustration $\Phi_{ex} = 0 \mod \Phi_0$, the minima are centered on $\delta_m = 0$ and are spaced by 2π in δ_p [Fig. 3.3b]. Along δ_m , there is only the one minimum at $\delta_m = 0$ [Fig. 3.3d], corresponding to no circulating current around the SQUID loop. Along δ_p for $\delta_m = 0$, the potential follows a $\cos \delta_p$ dependence. Thus, at unfrustration, the plaquette behaves like a single Josephson junction with critical current $2I_0$. When flux biased at $\Phi_0/2$, the plaquette exhibits a staggered pattern of energy minima about a line along δ_p for $\delta_m = \pi/2$ [Fig. 3.3c]. Figure 3.3e shows a linecut along a line between two adjacent minima as a function of δ_m ; the two minima correspond to opposite senses of circulating current around the plaquette loop, similar to a flux qubit [57] or fluxonium [54]. However, unlike these other qubits, these plaquettes also have another independent phase degree of freedom from δ_p , which corresponds to the phase drop across the plaquette. Along δ_p , the potential is simply $E_2 \cos 2\varphi$, with sequential minima separated by π [Fig. 3.3g], where the energy scale E_2 depends on the Josephson energies of the individual Josephson junctions E_J and the inductive energy of the SQUID loop inductance E_L .

While the behavior described here is generic for any dc SQUID, achieving a $\cos 2\varphi$ potential at frustration with a significant barrier height E_2 requires a sufficiently large ratio E_J/E_L . In the conventional language of dc SQUIDs, screening effects are characterized by the parameter $\beta_L = 2LI_0/\Phi_0 = E_J/\pi E_L$. For SQUIDs in the limit $\beta_L \to 0$ and perfect symmetry, the critical current of the SQUID will modulate to zero at frustration. For such a device, not only is the first-order Josephson energy suppressed, but E_2 will be vanishingly small as well, and thus not support bound states in a $\cos 2\varphi$ potential. In order to have a significant E_2 , E_J/E_L must be of order unity. The dc SQUID in Fig. 3.3 has $E_J/E_L = \pi$ to highlight the development of the π -periodicity at frustration.

We next consider deviations from this ideal π -periodic plaquette behavior. With the flux bias moved below (above) frustration, the π wells are raised above (below) the 0 wells [Fig. 3.4c]. To account for asymmetries between the two junctions in a plaquette we define

$$\alpha = (E_{J2} - E_{J1}) / (E_{J2} + E_{J1}), \qquad (3.2)$$

where $E_{J1}(E_{J2})$ is the Josephson energy of the left (right) junction. With a non-zero α , the common-mode potential along δ_p for $\Phi_{ex} = \Phi_0/2$ has equal minima for the 0 and π wells, but now the barrier heights between wells become asymmetric (Fig. 3.4d).



Figure 3.4: (a) Circuit schematic for dc SQUID plaquette with asymmetric Josephson junctions. Linecut between adjacent minima vs. δ_p for (b) $\Phi_{ex} = \Phi_0/2$, $\alpha = 0$, (c) $\Phi_{ex} = 0.45\Phi_0$, $\alpha = 0$, (d) $\Phi_{ex} = \Phi_0/2$, $\alpha = 0.05$.

Chapter 4

Plaquette: Layout, fabrication, and parameters

In this chapter, I give a description of the design, fabrication, and parameters of the device. The fabrication was done by my fellow graduate students, Yebin Liu and Brad Cole in our research lab at Syracuse University and the Cornell Nanoscale Facility.

4.1 Layout

In order to allow for local flux-biasing of the different plaquettes and charge-biasing of the various superconducting islands, our device incorporates a series of on-chip bias lines, indicated in Fig. 4.1. The heart of the device contains a chain of three plaquettes, each with two small Josephson junctions (115 nm \times 110 nm) and two junction-chain inductors (seventeen 140 nm \times 1070 nm junctions in series). Minimizing C_{isl} for each intermediate island between two adjacent plaquettes is critical for successful concatenation. Thus, ideally the four Josephson junctions in two adjacent plaquettes will all be located near the island between the plaquettes so that the junction electrode that is closest to the island will be as short as possible and contribute a minimal amount of excess capacitance to ground. However, in a chain of three plaquettes, this is only possible for one of the two intermediate islands. The other island will necessarily have to be connected to the two inductors for one of the plaquettes, and the capacitance to ground for these inductors will enhance the effective island capacitance (Fig. 4.2).




Figure 4.1: Schematic of chip entire chip on left. The pads along the perimeter are for wirebonding to the on-chip lines. PB01, PB12, PB23, and PB30 are the plaquette bias lines. SBC and SBO are two SQUID bias lines. CB1 and CB2 are the charge-bias lines for the islands between Plaquettes 1 and 2, and Plaquettes 2 and 3, respectively. CB_Sh is the charge bias line for the shunt capacitor. The microwave feedline is on the bottom of the chip. The readout resonator is the meandering line above it. The right image is zoomed in on the qubit. The large shunt capacitor dominates the lower half of the image, with the coupling capacitor to the readout resonator beneath it.



Figure 4.2: Circuit diagram of the three plaquette chain. To minimize C_{isl} for the island between Plaquettes 1 and 2 the Josephson junctions are all located near the island. However, it is not possible to simultaneously do the same for the island between Plaquettes 2 and 3.

In addition, the 3-plaquette chain has dummy plaquettes at either end, which have the same geometry as the other plaquettes, but the small junctions and inductorchain junctions are intentionally shorted out. The dummy plaquettes are included to symmetrize the geometry and minimize the inductive coupling of the on-chip flux-bias lines to the LC mode of oscillation of the plaquette chain, sometimes referred to as the M' coupling, as defined in Ref. [24].

There are four on-chip flux-bias lines for controlling the flux bias to each of the three plaquettes, with the labeling as in Fig. 4.3a. Each flux-bias line has a coplanar geometry and splits into a T-shaped path adjacent to the plaquette chain, with the two ends of the T connected directly to the ground plane. The plaquette bias lines are referred to as PB01, PB12, PB23, and PB30. The naming convention refers to which of the plaquette loops the bias line couple to strongly. So, PB12 couples primarily to Plaquette 1 and Plaquette 2, and does not couple to Plaquette 3 strongly. The 0 refers to one of the dummy plaquette loops on either end of the chain. In order to have a well-defined path for the return currents and to suppress slot-line modes between different portions of the ground plane, we fabricated superconducting ground straps across each flux-bias line in multiple locations. In addition to the flux-bias lines, we also have three charge-bias lines for tuning the offset charge to the shunt capacitor electrode, CB Sh, and each of the two intermediate islands between pairs of plaquettes, CB1 and CB2. These charge-bias lines are isolated from ground, but also include similar ground straps to the flux-bias lines. Figure 4.3 shows the layout of the plaqettes flux and charge bias lines.

Our design also includes a pair of series dc SQUIDs between the plaquette chain and C_{sh} that could be used for gate operations in a future implementation of a protected qubit based on concatenated π -periodic plaquettes. The two SQUIDs are controlled with two on-chip flux-bias lines that have the same T geometry as the plaquette lines. One line, *SBC*, is centered between the two SQUIDs and biases them equally. The second line, *SBO*, is offset so that it couples to one SQUID more strongly than the other, allowing for independent control of the two SQUIDs. These SQUIDs were not used in the present measurements and were maintained at a flux bias of $0 \mod \Phi_0$ throughout the experiment. At this bias point, the SQUIDs behave primarily as superconducting shorts, although we must still account for the nonlinearity of the SQUID junctions in modeling the energy levels for our device. The target shunt capacitance, $C_{sh} \sim 1000$ fF, for our present device is rather large compared to more conventional superconducting qubits. Nonetheless, in the present experiment, we followed the conventional approach typically used in superconducting qubits [58] and implemented C_{sh} with a planar superconducting Nb electrode with a small gap to the ground plane around the perimeter. To achieve such a large C_{sh} , the footprint of the capacitor electrode is considerably larger than for a transmon qubit.

For measuring our device, we have a coplanar waveguide (CPW) readout resonator with a fundamental resonance at 4.7 GHz. This is a 1/4-wave resonator with one end inductively coupled to a CPW feedline that is connected to our measurement circuitry; the other end of the resonator has a coupling capacitance $C_c = 36$ fF to our device.

The majority of our device is patterned in Nb, including the ground plane, bias lines, readout resonator, and shunt capacacitor. All Josephson junctions are fabricated from a standard $Al-AlO_x$ -Al double-angle shadow-evaporation process. As an initial attempt at superconductor gap engineering for reducing quasiparticle poisoning of the plaquette chain, we include two patches of Al for partially suppressing the Nb gap underneath – one patch is at the joint between the plaquette chain and the ground plane; the other patch is between the plaquette chain and shunt capacitor.

4.2 Fabrication

This device was fabricated on a high resistivity ($\geq 10 \text{ k}\Omega$ -cm) Si wafer that was given a standard RCA clean followed by an etch step in a buffered-2 per volume HF bath to remove native oxides immediately before loading into the vacuum chamber for the base-layer metal deposition. The base layer of 60-nm thick niobium is sputter-deposited and is then coated with DSK101-4 anti-reflective-coating (ARC) and DUV210-0.6 photoresist before performing deep-UV photolithography on a photostepper to define the ground plane, feedline, resonator, flux/charge bias lines, and the logical islands. The exposed wafer is then baked at 135°C for 90 seconds, developed with AZ 726 MIF, briefly cleaned with an ARC etch to remove any remaining unwanted ARC and then dry etched using a BCl₃, Cl₂, and Ar in an inductively coupled plasma etcher. The wafer is then subject to another buffered HF dip to remove any further oxides that may have formed on the surface of the remaining Nb or exposed Si.

The next set of lithography steps creates ground straps that connect regions of the



Figure 4.3: a) Microscope image of the plaquette chain. The three plaquette loops are false colored in red. Above and below the plaquettes are the dummy plaquettes that have no junctions in them. At the top of the image the chain connects to ground. The lead going off the bottom of the image goes to the two SQUIDs and the shunt capacitor. The four plaquette bias lines are false colored in blue. b) Zoomed-in image of the plaquettes. The island between Plaquette 1 and 2 (2 and 3) is false colored blue (red), along with its corresponding charge-bias line.

ground plane on either side of the flux, charge, and feedlines. The first step uses liftoff resist LOR3A and then DUV210-0.6 photoresist to expose a region underneath the intended ground straps where SiO₂ is deposited to function as an insulating dielectric support for the aluminum ground straps to follow. The SiO₂ is evaporated in an electron-beam evaporator at a rate 0.35 n/s until 100 nm is deposited. The wafer is then placed in 1165 Remover (N-Methly-2-pyrrolidone (NMP)) at 65°C to lift off the excess SiO₂ and resist and then another clean bath of 1165 Remover (NMP) at 65°C for further liftoff. The wafer is then sonicated for 10 seconds to remove any final remaining resist and SiO₂. The second layer of the ground strap process is exposed in the same way, using LOR3A and DUV photoresist, but this time the pattern is aligned over the existing SiO₂ and extends further so that once developed, there is an exposed region of the Nb ground plane for the Al to contact. The wafer is baked again and developed, and the ground straps are then deposited by electron-beam evaporation of Al (100 nm thick). The wafer is once again subject to NMP to remove the remaining resist and excess Al.



Figure 4.4: (a) A scanning electron micrograph of a pair of plaquette junctions. (b) An image of a chain of junctions for making a plaquette inductor.

Once clean, the wafer is put through a light oxygen plasma resist strip (Glen 1000) before a bilayer resist stack of MMA/PMMA is spun for electron-beam lithography to define the Josephson junctions. The Al-AlO_x-Al junctions are written at 100 keV, with a standard inline double-angle evaporation pattern. Following a brief ion mill step to remove native oxides on the exposed Nb regions, the junction electrodes are deposited with electron-beam evaporation. The bottom (top) electrode is 40 (80) nm thick. Once the junctions are deposited, the wafer is covered in S1813 photoresist and then diced to $(6.25 \text{ mm})^2$ chips. After the dicing, the aluminum metalization is lifted off and the chips are then cleaned with a UV/ozone process before measurement. Figure 4.4 shows images of the plaquette junctions and a junction chain for making a plaquette inductor.

4.2.1 rf SQUID resonator fabrication

The rf SQUID resonator presented in Chapter 5 was fabricated with a different style of inductors compared to the previous discussion in this chapter. Instead of relying on the Josephson inductance from chains of Josephson junctions, we use the kinetic inductance [59] from narrow traces of highly disordered superconducting thin films of granular Al (gr-Al) [60, 55, 61]. Similar to our plaquette-chain devices, this device is also fabricated on a high-resistivity Si wafer. These devices used a bilayer of Nb on top of granular aluminum, gr-Al that was sputtered in a single vacuum step. The first lithography pattern defines all of the features, including the rf SQUID loop, with a chlorine-based etch that etches both Nb and gr-Al. The second lithography step defines the nanowire inductors with a fluorine-based etch that selectively removes the Nb, while leaving the gr-Al, thus forming the gr-Al wires that make the compact inductors for the plaquette (Fig. 4.5). Additional photolighography steps create Nb ground straps that go over the flux lines and feedline to tie the ground plane together. Lifted off SiO₂ patches prevent the ground straps from shorting out the trace they are going over. The Josephson junctions are standard Al-AlO_x-Al tunnel junctions that are written with electron-beam lithography and deposited with a double-angle evaporation.

Although these rf SQUID resonators allowed us to successfully demonstrate a π -periodic plaquette, this approach for forming the inductors with gr-Al nanowires made it challenging to target particular inductance values. The gr-Al process is rather sensitive to the sputter conditions, and the kinetic inductance of the films tends to vary significantly over the area of a wafer. Thus, in our subsequent devices, we transitioned to using chains of Josephson junctions formed from conventional aluminum to form the inductors.



Figure 4.5: A scanning electron micrograph of a pair of granular aluminum nanowires. At the top of the image is the niobium on top of gr-Al. Beneath, the niobium has been selectively etched away leaving the gr-Al nanowire.

Chapter 5

Demonstrating π -periodicity

In this chapter, I describe our experiments with a plaquette embedded in an rf SQUID resonator in order to demonstrate the plaquette's effectiveness as a π -periodic element. The inductors for the device in this chapter were implemented with high kinetic inductance nanowires instead of junction chains discussed in other chapters.

5.1 rf SQUID

A conventional rf SQUID consists of a single conventional Josephson junction, with critical current I_0 , in parallel with an inductor, L_{rf} . The $\cos\varphi$ potential of the junction combined with the inductive energy from the inductor results in a flux-dependent inductance from the parallel combination of the junction and the inductor. By shunting the rf SQUID with a capacitor, it is possible to form a resonant circuit with a fluxdependent resonance frequency. Whether the potential is in a single- or double-well regime depends on the screening parameter β_L :

$$\beta_L = \frac{2\pi L_{rf} I_0}{\Phi_0}.$$
 (5.1)

We want a device in the low- β_L limit so that the resonance frequency is single-valued. The periodicity will be Φ_0 for such a conventional rf SQUID. In an rf SQUID, the phase across the junction is proportional to the total flux in the rf SQUID loop, consisting of the externally applied flux and the screening flux from the circulating current. By measuring the flux-modulation of an rf SQUID resonator, it is possible to determine the phase-periodicity of the junction potential. This ability is maintained when replacing the single Josephson junction with a plaquette. We will control the flux in the plaquette independently from the flux in the rf SQUID loop.



5.2 Device Layout

Figure 5.1: a) Circuit diagram of the device. b) Image of plaquette, with the two red lines indicating the flux lines for generating Φ_p and Φ_{rf} .

The device consists of an rf SQUID resonator that incorporates a plaquette. In order to maximize symmetry, the rf SQUID loop has a gradiometer design. Instead of a single junction, a plaquette is placed in the rf SQUID. This allows us to control the phase across the plaquette. A capacitor C_{sh} shunts the rf SQUID to create a resonant circuit. The resonator is capacitively coupled to a microwave feedline for readout. Both the plaquette and the rf SQUID inductors are made with granular aluminum. Granular aluminum is a disordered superconductor that we make by sputtering aluminum in the presence of oxygen. The kinetic inductance of this superconductor is a function of the normal state resistance R_n and the superconducting gap Δ , $L_K = R_n h/2\pi^2 \Delta$ [59, 55]. Two on-chip flux lines, I_{rf} and I_p , allow us to tune the flux through both the rf SQUID loop and the plaquette independently. To keep the design symmetric, there are also dummy flux lines, that are the mirror image of the real flux lines but terminate to ground away from the device.



Figure 5.2: Frequency scan of the transmission through the feedline for two different arbitrary flux points.

5.3 Flux Tuning

The frequency of the resonance tunes with both the flux through the rf SQUID loop and the plaquette loop (Fig. 5.2). Figure 5.3 shows the resonance frequency versus the two currents of the on-chip flux lines. For each flux-bias point, we measure S_{21} through the feedline as a function of frequency. We then identify the resonance frequency as the minimum of S_{21} . Yellow corresponds to unfrustation, around 6.18 GHz, while at frustration the resonance frequency tunes down by about 150 MHz. The gradient of the maxima from the bottom left to the top right is not periodic. We believe this gradient is due to the circulating current in the outer loop of the gradiometric rf SQUID approaching the critical current of the granular aluminum inductors. When this critical current is approached, the granular aluminum no longer behaves like a linear inductor and the inductance increases.



Figure 5.3: Tuning the bias currents for the rf SQUID and the plaquette. Color corresponds to the frequency of the resonator.

In Fig. 5.4, instead of the axes just being the bias currents, we have orthogonalized the fluxes using combinations of the two currents to scan pure fluxes Φ_p and Φ_{rf} in the plaquette and rf SQUID loops, respectively; the fluxes are expressed in units of Φ_0 . We can clearly see the modulation with the flux through the rf SQUID changes by a factor of two between plaquette frustration and unfrustration (indicated by red dashed lines).

Figure 5.5 shows the resonance tuning with the rf-SQUID flux at a) plaquette unfrustration and b) plaquette frustration. We clearly observe a switch from a periodicity of Φ_0 , corresponding to a $\cos \varphi$ dependence, to $\Phi_0/2$, corresponding to a $\cos 2\varphi$ dependence. Now that we have demonstrated a π -periodic element, we next quantify the purity of the π -periodic modulation. Imperfect π -periodic modulation



Figure 5.4: Frequency of the resonator tuning with the pure fluxes in the two loops. Dotted red lines mark plaquette unfrustration, $0 \Phi_0$ and frustration, $0.5 \Phi_0$.

can be caused by a residual E_1 term in the plaquette potential.

In Fig. 5.6a, we plot the extracted resonance frequency as a function of Φ_{rf} for $\Phi_p = \Phi_0/2$ with a quadratic fit to the resonance frequency maxima subtracted. This quadratic fit allows us to account for the gradient caused by the inductor nonlinearity due to screening currents in the outer gradiometer loop of the rf SQUID. Zooming in on the maxima (Fig. 5.6b), we see a spread of about 4 MHz. Comparing this to the total modulation of 150 MHz, we estimate an asymmetry of of 4 MHz/150 MHz $\sim 3\%$, implying that $E_1/E_2 \leq 0.03$. This residual E_1 can be caused by either not being at exact plaquette frustration or from asymmetries in the plaquette junctions or inductances. The rf SQUID resonator measurements only allow us to bound the residual E_1 level, but not to determine which of these possible sources is dominant.



Figure 5.5: a) Dependence of the resonance on the rf-SQUID flux at plaquette unfrustration. b) Dependence of the resonance on the rf-SQUID flux at plaquette frustration.



Figure 5.6: a) Modulation of the cavity frequency at plaquette frustration. b) Zooming in on the tops to see how much 2π or Φ_0 dependence remains.

Chapter 6

Measurement setup and flux tuning

In this chapter, I describe the measurement and characterization of the plaquette qubit device.

6.1 Experimental Setup

This device is measured on a BlueFors cryogen-free dilution refrigerator. The sample is mounted in a machined aluminum sample box (Fig. 6.1). The on-chip lines are wirebonded to copper traces in the box. These copper traces are soldered to SMA connectors on the outside of the box. The sample box is mounted on the mixing chamber stage of the fridge that has a base temperature of about 15 mK. Figure 6.2 is a schematic of the wiring of the fridge and the room temperature control electronics.

The entire inside of the fridge is under a vacuum. A large, room temperature mu-metal can sits in the vacuum can to shield the sample from external magnetic fields. Each of the temperature stages has a light-tight can that prevents light from the higher stage getting to the lower stages. There is also a Cryoperm magnetic shield that surrounds the cold-finger on the mixing chamber that acts as a second layer of magnetic shielding. Both the mixing chamber can and the Cryoperm are coated with an infrared absorbing layer made of a mixture of silica powder, fine carbon powder, and SiC grains in stycast epoxy [31]. This absorbs stray light that could break Cooper pairs on the device.



Figure 6.1: Machined Al sample box, Cu signal traces on Rogers board strips, soldered to SMA connectors at one end; Al wirebonds to device chip on other end. Machined Al lid not pictured.

6.1.1 Flux lines

Each flux line was connected to one channel of our BBN APSII arbitrary waveform generator (AWG). The APSII has a sampling rate of 1.2 GS/s and a ±1 V output with 14 bits of vertical resolution. 323 MHz gaussian filters and 32 MHz Mini-Circuits low-pass filters at room temperature keep noise from the AWG from getting to the sample. In the fridge, attenuators help to thermalize the line at each temperature stage. The total attenuation, 20 dB, was chosen so that the ±1 V range of the AWG would be a able to cover a bit over two Φ_0 periods in each loop. Ideally, one would place all of the attenuation at the lowest temperature stage possible in order to attenuate thermal noise from higher stages. However, since the attenuators dissipate heat, putting an excessive amount of attenuation on the mixing chamber



Figure 6.2: Schematic of the fridge wiring. Dashed lines are set up identically to the solid line they are grouped with.

would heat up the sample. Instead, we distribute the cold attenuators on the still and 3 K stages, which have greater cooling power than the mixing chamber. Finally, before connecting to the sample box, the flux lines go through 1.3 GHz Mini-Circuit low-pass filters and eccosorb filters on the mixing chamber.

6.1.2 Charge lines

Each of the three charge lines has a 20 dB T-style attenuator on the 3K stage of the fridge that acts as a voltage divider. There is a 10 k Ω resistor at room temperature that was chosen to make the total voltage division 1000:1. An SRS SIM928 isolated voltage source is used to set the voltage on the bias line. The resistor to ground for the voltage divider is on the 3K stage to limit Johnson noise in the resistor that would introduce offset charge bias noise to the qubit. Each line also has a 80 MHz Mini-Circuits low-pass filter and eccosorb filter on the mixing chamber that limits high frequency noise from higher temperature stages. The charge bias line for the shunt capacitor also has an Anritsu K250 bias-T on the mixing chamber that allows a microwave tone to be applied to the qubit in order to drive transitions between levels.

6.1.3 Microwave lines

The fridge has one microwave input and output for driving and reading out the qubit's readout resonator. To drive the resonator, a tone from a microwave generator (LO) is mixed with a 13 MHz waveform produced by an AWG. This signal goes into the fridge, where it passes through a total of 49 dB of attenuation, an 8 GHz high-pass KL filter, and a high-pass eccosorb filter before reaching the device. The attenuation and filters act to reduce the noise from higher temperature stages and room-temperature electronics.

After the signal passes through the feedline on the chip, it is routed through another set of eccosorb and KL filters, two 4-8 GHz microwave isolators, and a Low Noise Factory high-electron-mobility transistor (HEMT) amplifier. The filters and isolators reduce the amount of noise from room temperature and the HEMT that reaches the device. At room temperature, the signal goes through more amplification and then is mixed down with the LO to 13 MHz. This 13 MHz signal is then digitized. The digitized signal is then processed to discriminate the dispersive shift of the readout resonator that depends on the state of the device, similar to the readout of conventional superconducting qubits.

6.2 Flux Tuning and Orthogonalization

The device has a total of five SQUID loops and six on-chip bias lines. This means that we can independently tune the flux in each of the loops as long as we can account for all the different mutual inductances between the bias lines and SQUID loops. Figure 6.3 shows the readout cavity modulating as the voltage on the PB12flux line is tuned. The voltage is applied by an AWG channel at room-T, then the configuration of attenuation in the fridge determines the amount of current that flows through the flux line for a given voltage. When the flux through one of the SQUID loops approaches frustration, the resonant frequency of the cavity will decrease due to the increased inductance shifting the qubit frequency lower. Since PB12 has large mutuals to both Plaquettes 1 and 2, as well as a smaller mutual to Plaquette 3, it is difficult to tell from this scan which dip in frequency corresponds to which of the SQUID loops being frustrated.

In order to get a better handle on the multi-dimensional flux space of the device, we can look at two-dimensional flux scans. These scans are done by driving at a fixed cavity frequency that is near the resonant frequency of the cavity when one of the loops is frustrated. This drive results in high transmission through the feedline when the plaquettes are away from frustration, while near frustration, we are driving on resonance and get low transmission through the feedline. The two SQUID switch loops are easier to distinguish because they are spatially separated from the plaquette SQUIDs, and thus have smaller cross mutual inductances to the plaquette loops. Figure 6.4 shows the modulation of the cavity as we vary the voltage on both of the SQUID switch flux lines. The blue lines of two different slope correspond to frustration for each of the SQUID loops in the SQUID switch; crossing blue lines occur when both SQUID loops are simultaneously frustrated. For the upcoming spectroscopy measurements in the following chapter, both SQUIDs in the SQUID switch will be continually biased at unfrustration so that the SQUID switch has a minimal impact on the level spectrum.

Figure 6.5 shows two examples of tuning different pairs of plaquette bias lines.



Figure 6.3: Cavity response from tuning one of the flux bias lines. This is a measurement of S_{21} through the feedline, and the colorscale is the magnitude of S_{21} .

We see that there are three sets of blue lines that correspond to frustration for the three plaquette loops. Two of the lines crossing correspond to double frustration for a pair of plaquettes and the intersection of all three corresponds to triple frustration. The period between a given set of parallel lines is 1 Φ_0 for that particular loop. The identification of the different frustration lines with each plaquette can be deduced by the relative mutual inductances to the bias lines. For example, the nearly vertical lines in Fig. 6.4a belong to Plaquette 1 because they tune rapidly with *PB*01, which is close to Plaquette 1, and minimally with *PB*30, which is far away. From the various periods and slopes of these lines, we can calculate the mutual inductance matrix,

$$\vec{\Phi} = \mathbf{L}\vec{I} + \vec{x},\tag{6.1}$$

where $\vec{\Phi}$ is a length 3 vector of the plaquette fluxes, \vec{x} is a length 3 vector of the



Figure 6.4: Tuning the two SQUID switches with the two on-chip lines. The two sets of blue lines correspond to frustration for the two SQUID switches. This is a measurement of S_{21} through the feedline at a frequency corresponding to the frequency of the cavity near SQUID frustration, and the colorscale is the magnitude of S_{21} .

flux offsets to each plaquette at zero bias, \vec{I} is a length 4 vector of the plaquette bias currents, and L is a 3×4 matrix of the mutual inductances. The flux offsets at zero bias are due to small background magnetic flux that gets trapped in place when the ground plane goes superconducting during the initial cooldown of the device. These offsets can be stable for weeks at a time, although small changes that necessitate recalibration can occur, often corresponding to when something is changed with the room-temperature electronics. For the experiments that we will be doing we will need to be able to control the fluxes to within less than $1 \text{ m}\Phi_0$. The resolution of these scans is not great enough to get the flux offsets and mutuals to that accuracy. To try to achieve greater accuracy we can zoom in on one of the double frustration points (Fig. 6.6). Here we see fine structure symmetric around frustration that we can use to very accurately find the flux offsets for two of the plaquettes. This structure comes from higher levels of the device crossing the cavity when a plaquette is tuned near frustration (Fig. 6.7). By getting the locations of double frustration with high accuracy from these fine scans, we can calculate the flux periods and the slopes in order to get the inductances with the required precision. Table 1 shows the measured mutual inductance matrix and how it compares to the inductance matrix obtained from simulating the layout with the numerical software package InductEx [62].



Figure 6.5: Scanning different combinations of the plaquette flux lines. Measuring feedline transmission. Colorscale corresponds to $|S_{21}|$ at a fixed frequency near the readout cavity resonance. The three sets of parallel blue lines correspond to frustration for the three plaquettes. a) *PB*01 vs *PB*30. b) *PB*12 vs *PB*23. c) Picture of on-chip flux lines and plaquettes.

Using this matrix, we can now apply combinations of voltages to cancel out crosstalks and take steps in the pure flux direction for any plaquette or combination of plaquettes. Figure 6.8 again shows Plaquette 1+2 double frustration, but now the fluxes have been orthogonalized and the axes are stepping through the pure fluxes through Plaquette 1 and 2 while the flux in Plaquette 3 is held constant.

Simulated Inductance Matrix (pH)									
	<i>PB</i> 01	<i>PB</i> 12	PB23	PB30					
Plaq1	0.59	0.76	-0.17	0.11					
Plaq2	0.15	-0.69	-0.55	0.24					
Plaq3	0.07	-0.02	0.60	0.76					
Extracted Inductance Matrix (pH)									
	PB01	PB12	PB23	PB30					
Plaq1	0.639	0.660	-0.146	0.053					
Plaq2	0.201	-0.661	-0.539	0.155					
Plaq3	0.134	-0.244	0.674	0.591					

Table 1: Simulated and measured plaquette flux line inductance matrix, L (Equation 6.1). Simulated inductances using InductEx for our chip layout.



Figure 6.6: Taking fine flux-bias steps with PB01 and PB12 near Plaquette 1+2 double frustration. Measuring feedline transmission. Colorscale corresponds to $|S_{21}|$ at a fixed frequency near the readout cavity resonance.



Figure 6.7: Simulation of the energy-level spectrum of the qubit-plus-readout resonator system near Plaquette 2 frustration, zoomed in near the resonator's frequency. The horizontal line at 4.7 GHz is the readout resonator. The other lines are various heavy fluxon transitions of the qubit that we can see cross the resonator near frustration thus leading qualitatively to the type of fine-structure that we observe in high-resolution scans of the readout resonator, as in Fig. 6.6. the modeling of the energy-level spectrum will be described further in Chapter 7.



Figure 6.8: Taking fine steps in the pure Plaquette 1 and Plaquette 2 directions, centered on Plaquette 1+2 double frustration. Measuring feedline transmission. Colorscale corresponds to $|S_{21}|$ at a fixed frequency near the readout cavity resonance.

Chapter 7

Plaquette Spectroscopy Measurements

In this chapter, I show device spectroscopy and compare the spectroscopy in the vicinity of the different single, double, and triple frustration points. The spectroscopy tone is summed with the shunt capacitor charge bias line using a bias-T mounted on the mixing chamber (Fig. 6.2). Because of the large frequency range we are interested in, including frequencies much lower than traditional qubits are operated, we are creating the spectroscopy pulses by gating a generator with a fast microwave switch rather than using an IQ mixer (Fig. 6.2).

7.1 Plaquette Initialization

Before each spectroscopy/readout pulse, we initialize the circuit in the π well by setting the plaquette flux bias to 0.1 Φ_0 away from frustration; we then ramp the flux bias to the flux coordinates on the flux axis with a gaussian edge with a 167 ns standard deviation, idle for 5 μ s, then apply a 5 μ s spectroscopy tone, and then a 5 μ s cavity measurement pulse. (Fig. 7.1).

We initialize 0.1 Φ_0 away from frustration for 30 μ s so that we are far enough away such that there is only one well in the potential while not going farther than is needed, as the larger the pulse, the larger the distortions of the pulse that reaches the device. We chose to initialize for 30 μ s by increasing the time spent idling at the initialization point until the population in the desired well saturated. We use a



Figure 7.1: Schematic of pulse sequence for spectroscopy measurements. The blue line represents the flux of the plaquette, The red line shows the timing of the spectroscopy pulse. The yellow line shows the timing of the measurement pulse.

167-ns gaussian edge pulse shape so that we are moving fast enough to be adiabatic but not so fast that there are fourier components at the qubit frequency that could unintentionally excite the qubit. We found that a 167-ns gaussian edge was fast enough to be adiabatic by preparing the qubit in the π well, bringing the qubit across frustration where the 0 well is the minimum, measuring, and observing that the qubit stayed in the π well. The 5 μ s idle before the spectroscopy tone is applied provides time for the flux to settle. These distortions can be caused by impedance mismatches on the line and eddy currents in the normal copper traces in the sample box [63]. It is possible to measure these distortions and compensate for them [64], but for the measurements we are doing here, the short idle is adequate. We determined this by varying the idle time, and by 5 μ s the spectroscopy had settled to an asymptotic level.

7.2 Single Frustration

For performing spectroscopy near single frustration of any of the three plaquettes with the remaining two plaquettes maintained at unfrustration, we drive a microwave probe tone into the charge bias line coupled to C_{sh} then read out the dispersive shift of the cavity. Before each spectroscopy/readout pulse, we initialize in the π well as described above; we then quickly ramp the flux bias to $\Delta \Phi = \Phi - \Phi_0/2$, which is the flux coordinate specified in our various spectroscopy plots and apply the spectroscopy tone. For scans near Plaquette 1 and 2 single frustration, the flux is then brought with square pulse to a common readout point of 10 m Φ_0 to the right of frustration. For scans near Plaquette 3 single frustration, we read out at the same flux point as the spectroscopy because we need to overlap the spectroscopy pulse with the readout pulse near Plaquette 3 frustration. We believe this is due to the qubit having a T_1 that is short compared to the readout pulse when Plaquette 3 is near frustration. For all the spectroscopy scans, we are plotting the quadrature distance between the measurement of S_{21} through the feedline with and without a spectroscopy tone.

For example, Fig. 7.2 shows single-frustration spectroscopy measurements for Plaquette 2. The features that disperse gradually with flux correspond to the plasmon excitations within the π well where the qubit is initialized (as discussed in Fig. 3.2); in addition to the 0-1, 0-2, and 0-3 transitions, we also observe transitions out of the first excited state in the well, such as 1-2, 1-3, 1-4, due to insufficient initialization into the ground state and excessive spurious excitation. These excitations out of the ground state are most likely related to the low energy scale of the plasmon transitions, which at ~ 800 MHz are comparable to the frequency scale of the thermal background of the qubit environment; additionally, the large area of our shunt capacitor will support quite low-frequency spurious antenna modes, which can absorb photons from the qubit environment and drive unwanted qubit transitions [65]. Although we are unable to prepare fully in the ground state of the π well, we only observe weak transitions out of the 0 well, indicating that our initialization is predominantly preparing the circuit in the π well. Besides the plasmon features, we also observe heavy fluxon transitions that disperse linearly with flux, and with a much steeper slope than the plasmons, that arise from transitions between levels in the π and 0 wells. We observe qualitatively similar behavior for single frustration of Plaquettes 1 and 3 (Fig. 7.3).

The curves included in Fig. 7.3 are generated from a detailed numerical modeling of the energy levels done by my fellow graduate student Yebin Liu using the SuperQuantPackage developed by our theory collaborator, Andrey Klots [66]. The circuit is divided into a series of independent harmonic oscillator coordinates and cyclic coordinates corresponding to islands with quantized charge connected to Josephson junctions. We express the device Hamiltonian in this basis and numerically diagonalize to extract the energy eigenvalues. With the ability to calculate the level spectrum,



Figure 7.2: Spectroscopy as a function of flux at Plaquette 2 single frustration. We are plotting the quadrature distance between the measurement of S_{21} through the feedline with and without a spectroscopy tone.

we then adjust the various circuit parameters to fit the measured transitions from the spectroscopic data; the various fit parameters will be defined later in this section. We observe excellent agreement for the fits, including capturing the splittings that result when a fluxon crosses a plasmon due to the resonant tunnel coupling between aligned levels in the 0 and π wells.

These splittings at the plasmon/fluxon crossings depend on the offset charge on the C_{sh} island due to an analogue of Aharonov-Casher interference [18, 53] between tunneling paths forward or backwards by π in the $\cos 2\varphi$ potential. This charge modulation is most prominent for splittings near the top of the barrier between the wells, which is close to the readout cavity frequency (Fig. 6.7). Thus, this charge tuning is most easily seen in the periodic charge modulation of the cavity dispersive shift (Fig. 7.4). The random shifts of the periodic modulation with offset charge bias correspond to changes in the total offset charge coupled to the island. The offset charge changing with time reflects the charge configuration near the device changing and can be related to microscopic two level systems (TLS) on the surfaces of the device or gamma ray impacts from background radioactivity [67, 68]. High energy particles impacting the device generate a large number of electron-hole pairs in the Si substrate, which diffuse based on the band structure, then get trapped in defects, thus causing a change in the local charge environment. We see the offset charge jump on average every few minutes. This is not unreasonable, given that the physical size of the shunt capacitor makes its charge sensing area quite large. At single frustration, as expected, the dispersion of the heavy fluxons is linear down to zero energy, thus offering no protection against flux noise. Because only one plaquette is frustrated here, there is no concatenation, and, thus, no light fluxons (as discussed in Sec. 3.1).

Table 2 contains the parameters that resulted from the spectroscopy fits and were used for the modeled transition frequency curves in Fig. 7.3. E_J is the Josephson energy of one of the conventional small Josephson junctions in each plaquette, E_C is the charging energy of each small junction, E_L is the inductive energy of the junction chain, and C_{sh} is the value of the shunt capacitance. $E_{CL} = 2e^2/C_{CL}$ accounts for the charging energy of the junction chain inductors; C_{CL} is the capacitance of one of the junctions in the chain divided by 17 to account for the 17 junctions in series that make up the chain. α is a measure of the asymmetry of the two small junctions of the plaquette (Eq. 3.2). L_{factor} accounts for the inductance of the unfrustrated plaquettes



Figure 7.3: (a) Zoomed-in optical micrograph of plaquette chain showing labeling of plaquettes. Spectroscopy as a function of flux near (b) Plaquette 1 single frustration, (c) Plaquette 2 single frustration, and (d) Plaquette 3 single frustration, prepared in the right(π) well. Lines indicate modeled transitions from the spectroscopy fitting process with the following scheme: red lines are plasmon transitions, blue lines are fluxon transitions; dotted lines are transitions out of the 0_R state; dash-dotted lines are transitions out of 2_R the state.

that are in series with the frustrated plaquette. We find that in addition to fitting the data to better than 10% of the measured transition frequencies, the fitted parameters agree well with what we expected based on our design and fabrication. The agreement between the Plaquette 1 and 2 fit parameters and expected values is quite good. For



Figure 7.4: Initializing the qubit in the π -well and repeatedly scanning the shunt capacitor bias line while reading out the cavity 16 m Φ_0 away from Plaquette 2 single frustration, where the charge dependence is particularly strong. At this flux, a higher qubit level with a large charge sensitivity is near the readout cavity and thus strongly coupled, causing a large dispersive shift.

plaquette 3, the agreement is also reasonable, but not as good as for Plaquettes 1 and 2 and we are continuing to investigate the larger discrepancy for Plaquette 3.

7.3 Double Frustration

Now we are initializing in the π wells for two of the plaquettes simultaneously, as described in Section 7.1, then scanning the flux point for the spectroscopy along a vector in the direction from where the 0 wells of both plaquettes are the minimum (00) to where the π wells for the two plaquettes are the minimum ($\pi\pi$). The local

	E_J	E_C	E_L	E_{CL}	C_{sh}	0	T.
	(K)	(K)	(K)	(K)	(fF)	α	Lfactor
Plaquette 1	1.65	3.65	1.12	5.6	1155	0.03	1.08
Plaquette 2	1.65	3.67	1.11	6.36	1190	0.02	1.05
Plaquette 3	1.97	4.00	1.27	6.66	1443	0.04	0.91
Estimated	1.45	4.4	1.39	7.1	1000	0.02	1
parameters							

Table 2: Single frustration fitted parameters and estimated parameters from design and fabrication tests.

flux biasing will allow us to perform spectroscopy at the three different plaquette combinations for double frustration. This will allow us to study the effectiveness of concatenation for the different plaquette combinations.

When we are near double or triple frustration, the energy levels will also become sensitive to the offset charge on the superconducting islands between the frustrated plaquettes. Similar to the charge-modulation at single frustration with the offset charge bias to the C_{sh} island, this is also an effect that is analogous to Aharonov-Casher interference, now in the two-dimensional space formed by the phases across the two frustrated plaquettes. Figure 7.5 shows one example of measuring spectroscopy at Plaquette 1+2 double frustration without doing any type of charge stabilization where there was a jump in the offset charge on the island between the plaquettes during the measurement. It is difficult to compare the data before and after the jump. To get self-consistent data, we are going to need to stabilize the island charge offset before we measure. For longer spectroscopy measurements, we will need to run a brief calibration scan to stabilize the offset charge on the intermediate island(s) on a timescale faster than the typical time between these offset charge jumps.

Figure 7.6 shows measurements at various double frustration points, as well as triple frustration, where we are tuning the two island charge biases while applying a microwave tone on the 0-1 transition for each particular frustration point. The two charge-bias lines are for controlling the offset charge bias of each of the two islands, but there will be crosstalk for each of these to the other island. The clear charge tuning for the intermediate islands is evidence for effective hybridization and



Figure 7.5: Spectroscopy around the 0-1 plasmon transition near Plaquette 1+2 double frustration. There is an abrupt change part way through the scan when the offset charge jumps on the intermediate island between Plaquettes 1 and 2.

implementation of stabilizers. Each of the quadrants shows a different combination of frustrated plaquettes. Figure 7.6a shows Plaquette 1+2 double frustration, where we see a clear modulation that is faster with the island 1 bias line. At Plaquette 2+3 double frustration (Fig. 7.6b), we see a faster modulation because the placement of the junctions makes the island between Plaquettes 2 and 3 larger than that between 1 and 2. At 1+3 double frustration (Fig. 7.6c), the island is now even bigger and we see a faster modulation, especially with the island 1 bias line. Using the slopes and periods of these modulations, we can extract the capacitance matrix between the charge bias lines and the plaquette islands (Table 3). These extracted values agree reasonably well with the Q3D simulations of our device's geometry [69]. At triple frustration (Fig. 7.6d), we see two separate modulations with different slopes and


periods, consistent with simultaneous tuning of the offset charge on the two different intermediate islands.

Figure 7.6: Scanning the Island 1 and Island 2 charge lines for: (a) Plaquette 1+2 double frustration, (b) Plaquette 2+3 double frustration, (c) Plaquette 1+3 double frustration, and (d) Plaquette 1+2+3 triple frustration.

As the islands between the plaquettes are significantly smaller than the shunt capacitor, we expect the offset charge to be much more stable because of the smaller charge sensing area. In order to measure both offsets nearly simultaneously, we first scan Island 1 charge with Plaquettes 1 and 2 frustrated while Plaquette 3 is 50 m Φ_0 away from frustration; we then shift the fluxes slightly and scan Island 2 charge while Plaquettes 2 and 3 are frustrated and Plaquette 1 is 50 m Φ_0 from frustration. Figure 7.7 shows the results of repeatedly running this procedure over 11 hours. As expected, given its relatively smaller size [67, 68], the offset charge on the island between Plaquettes 1 and 2 is more stable than the island between Plaquettes 2 and

Simulated capacitance matrix (aF)									
	CB_Sh	CB1	CB2						
Isl_{sh}	57	419	353						
Isl_1	0	45	12						
Isl_2	0	27	88						
Extracted capacitance matrix (aF)									
	CB_Sh	CB1	CB2						
Isl_{sh}	57	501	327						
Isl_1	0	70	12						
Isl_2	0	73	120						

Table 3: Simulated and measured plaquette island charge line capacitance matrix. Simulated capacitance values are obtained with the Q3D numerical software package.

3. However, both are relatively stable over the period of about half an hour.

Now we can use the ability to stabilize the intermediate island offset charge to investigate the flux-dependence of spectroscopy near the various double frustration points. Approximately every twenty minutes, we run a scan of the intermediate island charge that takes about 30 seconds. We fit this with a cosine to find the appropriate charge bias to apply to keep the offset charge on the intermediate island constant. Figure 7.8 shows a spectroscopy scan for double frustration of Plaquettes 1 and 2 where we were doing this charge stabilization periodically throughout. We see similar plasmon transitions as in the single frustration measurements. However, unlike single frustration, where the suppressed tunneling between the $0/\pi$ wells allows the device to remain in the π well where it was prepared even after the flux is ramped well past frustration, at double frustration, the large gap between the symmetric and antisymmetric levels Δ_{SA} causes the device state to transition adiabatically from $\pi\pi$ to 00 upon passing through double frustration. At higher frequencies, we directly observe the steeply dispersing light fluxon transitions, with the minimum at double frustration corresponding to Δ_{SA} from hybridization of the 00 and $\pi\pi$ wells of the two frustrated plaquettes. Observing hybridization and the flattening of the energyband dispersion is characteristic of a stabilizer between the two plaquettes. The blue modeled transition curves on the plot in Fig. 7.9b indicate the heavy fluxon



Figure 7.7: Simultaneous measurements of Island 1 and 2 charge offsets over an 11-hour span. Details on the particular measurement sequence here can be found in the text.

dispersion, between the lowest levels of the $00 + \pi\pi$ and $0\pi + \pi 0$ wells in this case, which no longer extend linearly to zero energy at frustration. Instead, the heavy fluxons exhibit a quadratic curvature, characteristic of effective hybridization of the two plaquettes.



Figure 7.8: Spectroscopy as a function of flux at Plaquette 1+2 double frustration.

As with the spectroscopy at single frustration, we include curves for the various transitions from our numerical modeling and fitting for double frustration for Fig. 7.9. In this case, the larger Hilbert space at double frustration requires a significant increase in computational resources. Our modeled transition curves agree well with the measured spectroscopy, properly capturing the plasmon and heavy fluxon transitions, as well as the light fluxons to the antisymmetric levels. We observe that the effectiveness of concatenation depends on C_{isl} of the intermediate island between the two frustrated plaquettes. For double frustration of Plaquettes 1 and 2 [Fig. 7.9(b)], the symmetric-antisymmetric gap is 2.8 GHz. By contrast, at double frustration of Plaquettes 2 and 3 [Fig. 7.9(c)], which have a significantly larger C_{isl} because of the



Figure 7.9: (a) Optical micrograph of device with labeling of plaquettes in chain. Spectroscopy as a function of flux at (b) Plaquette 1+2 double frustration, (c) Plaquette 2+3 double frustration, and (d) Plaquette 1+3 double frustration. Lines indicate modeled transitions with the following scheme: red = plasmons, blue = heavy fluxons, purple = light fluxons, black = cavity-assisted transitions, dotted = transitions out of 0 level, dashed = transitions out of 1 level, solid = transitions out of 2 level.

orientation of the junction chain inductors for Plaquette 2, we observe a much smaller Δ_{SA} of 1.1 GHz and a correspondingly larger curvature of the heavy fluxon transition. Double frustration of Plaquettes 1 and 3 [Fig. 7.9(d)] results in an even smaller

 Δ_{SA} of 0.5 GHz because of the excess capacitance to ground of the unfrustrated Plaquette 2. The variation of Δ_{SA} with E_C^{isl} is summarized in Fig. 7.10, which shows the experimentally measured values for Δ_{SA} for the three different double frustration combinations, as well as numerically modeled Δ_{SA} values for a range of E_C^{isl} . Effective concatenation and a significant Δ_{SA} thus requires E_C^{isl} to be at least a few K.



Figure 7.10: Plot of Δ_{SA} and curvature of fluxon transition between even/odd-parity ground states vs. E_C^{isl} showing measured values for Plaquette 1+2, 2+3, and 1+3 double frustration (solid triangles) as well as modeled values for a range of C_{isl} (open circles), plus Plaquette 1+2 parameters but with $E_C = 4$ K.

Looking more closely at the 0-3 plasmon transition near Plaquette 1+2 double frustration, we can observe the dependence of the levels on the intermediate island offset charge (Fig. 7.11a). There are clearly two parity bands visible, 180° out of phase with each other. This is due to quasiparticles, which have a charge of 1e, tunneling on and off the intermediate island between Plaquettes 1 and 2 at a faster rate than we can measure so that we average both the even and odd parity states together. We see



Figure 7.11: (a) Spectroscopy of the 0-3 plasmon transition versus the Charge Island 1 bias, 17 m Φ_0 to the right of Plaquette 1+2 double frustration. There are clearly two parity bands visible, 180° out of phase with each other, indicating the presence of fast quasiparticle poisoning on the intermediate island between Plaquettes 1 and 2. The red and blue dotted lines are the fitted transition that correspond to different quasiparticle parity on the intermediate island between Plaquettes 1 and 2. (b) Spectroscopy of the 0-3 plasmon transition versus the Charge Island 2 bias, 11 m Φ_0 to the right of Plaquette 2+3 double frustration with fitted transitions.

similar fast quasiparticle poisoning at Plaquette 2+3 double frustration (Fig. 7.11b). The data and the fits show reasonable agreement. Excess quasiparticle generation is likely due to spurious antenna modes of the large shunt capacitor leading to the absorption of pair-breaking photons that create large currents in the plaquette junctions that generate quasiparticles on the intermediate islands [65, 70]. This is an important issue that needs to be solved for eventually making an effective charge-parity qubit.

Table 4 contains the parameters that went in to the fits for Figure 7.9. We again find that in addition to fitting the data to better than 10% agreement, the fitted parameters agree well with what we expected based on our design and fabrication. The fit values of C_{isl} for both intermediate islands from the fits to the measured double frustration spectra for Plaquettes 1+2 and 2+3 are not so far off with our separate finite-element method numerical modeling of the device capacitances, and the

	$\begin{array}{c c} E_J \\ (K) \end{array}$	E_C (K)	$\begin{array}{c} E_L \\ (\mathrm{K}) \end{array}$	$\begin{array}{c} E_{CL} \\ (K) \end{array}$	$\begin{array}{c} C_{sh} \\ (\text{fF}) \end{array}$	α	$\begin{array}{c} C_{isl} \\ (\text{fF}) \end{array}$	L_{factor}
$\begin{array}{c} \text{plaquette} \\ 1/2 \end{array}$	1.75	3.54	1.2	6.34	1241	0.03	1.52	0.99
$\begin{array}{c} \text{plaquette} \\ 2/3 \end{array}$	1.76	3.53	0.9	7.4	1287	0.04	5.68	1.03
plaquette 1/3	1.73	3.48	0.90	6.62	1308	0.03	8.139	0.98
Estimated parameters	1.45	4.4	1.39	7.1	1000	0.02	Vary	1

Table 4: Double frustration fitted parameters and estimated parameters The estimated C_{isl} for Plaquette 1+2 and 2+3 double frustration are 1.17 and 3.1 fF.

different island capacitances scale correctly for the different plaquette combinations. All of the double frustration fits, including those that include Plaquette 3 (2+3 and 1+3) capture the E_J , E_L , E_C , C_{shunt} , etc. values that are more consistent with our estimated parameters compared to the Plaquette 3 single frustration fits (Table 2).

7.3.1 Triple Frustration

By simultaneously frustrating all three plaquettes, we measure spectroscopy in the vicinity of triple frustration while initializing in $\pi\pi\pi$ and scanning the flux along a line from 000 to $\pi\pi\pi$ (Fig. 7.12). In this case, we are unable to use our numerics to fit the level spectrum since the size of the Hilbert space becomes prohibitively large. Nonetheless, we are able to compute the spectrum using our averaged parameter values from earlier fits to 1+2 and 2+3 double frustration and single frustration of the plaquettes ($E_J = 1.7$ K for all three plaquettes, $E_L = 1.1$ K for Plaquettes 1 and 2, $E_L = 0.9$ K for Plaquette 3, $E_C = 3.6$ K, $C_{sh} = 1195$ fF, $E_{CL} = 6.1$ K for Plaquettes 1 and 2, $E_{CL} = 6.4$ K for Plaquette 3, $\alpha = 0.03$, $L_{factor} = 1.2$). We again obtain good agreement with the measured transitions. In particular, the heavy fluxon transitions have even less curvature than for double frustration, and follow a cubic dispersion. Figure 7.6d, shows the two-dimensional scan of the two intermediate island charge-bias lines. We observe modulation with two different periods and slopes



Figure 7.12: Spectroscopy as a function of flux at triple frustration. Lines indicate modeled transitions with the following scheme: red = plasmons, blue = heavy fluxons, purple = light fluxons, dotted = transitions out of 0 level, dashed = transitions out of 1 level, solid = transitions out of 2 level.

corresponding to the separate tuning of the offset charge on each intermediate island. This is double Aharonov-Casher interference for the different tunneling paths in the space of the phases across the three plaquettes due to variations in the offset charge on the two intermediate islands.

7.3.2 Outlook

While our present device successfully demonstrates the implementation of a stabilizer term in superconducting hardware with the concatenation of multiple plaquettes, we are not able to operate it as a qubit due to spurious excitations out of the ground state and fast quasiparticle poisoning. The flattening of energy bands with successful concatenation and the observation of three different types of Aharonov-Casher interference from charge modulation of various spectral gaps are evidence that the stabilizer terms in the Hamiltonian are present. The success of our modeling of measured transitions and our direct measurements of Δ_{SA} let us calculate the ideal set of parameters to target higher energy levels of the excited states while maintaining the stabilizer term. This will make us less susceptible to noise and reduce spurious excitations and allow us to perform a more complete initialization into the ground state.

Chapter 8

Conclusions and Future Work

8.1 Conclusions

By embedding a plaquette in an rf SQUID, we were able to demonstrate the π -periodic phase dependence of the plaquette. We showed that at plaquette frustration we were able to suppress E_1/E_2 to 3%.

We mapped the flux space of our 3-plaquette chain device. We measured the flux and charge dependence of the the device's energy levels with microwave spectroscopy. We observed a softening of the energy band dispersion with respect to flux that is exponential in the number of frustrated plaquettes that corresponds to the device being protected against errors caused by dephasing due to flux noise. This, along with our observation of three different types of Aharonov-Casher interference from charge modulation of various spectral gaps, are evidence that the stabilizer terms in the Hamiltonian are present. The flattening of the energy band dispersion with respect to flux in combination with the large shunt capacitance show promise of being able to achieve a qubit design with simultaneous protection from both phaseand bit-flip errors.

8.2 Further Development of Protected Charge-Parity Qubits

While our present device successfully demonstrates the implementation of a stabilizer term in superconducting hardware, the development of a protected qubit based on the hybridized ground states of opposite parity will require larger energy scales for the

excited states. Combined with weaker radiative coupling to parasitic high-frequency modes from a more compact C_{sh} , perhaps implemented with a parallel-plate rather than planar design, this will avoid excessive spurious transitions to excited states. The lowest-frequency antenna mode of the shunt is roughly set by one wavelength matching the perimeter of the shunt capacitor [65]. The antenna modes of the shunt couple strongly to free space and allow the device to absorb stray radiation. The perimeter of our device is approximately 7 mm. In the presence of the Si substrate, this corresponds to a fundamental antenna frequency of about 17 GHz. A parallelplate design would be problematic for a transmon, because of the significant increase in dielectric loss for a deposited dielectric. This is not much of an issue for our qubit, where the computational states are formed from the ground state doublet with quite small matrix elements of the charge operator for transitions between the two states. Even though the loss tangent of a deposited dielectric will be significant, the extremely low frequency of the ground-state doublet splitting, combined with the quite small matrix element of the charge operator between the states of the doublet, leads to $T_1 \gg 1$ s. A device with higher excited-state energies requires larger E_J and E_L , ideally at least 4 K. At the same time, we must maintain a large E_C in order to also have a large Δ_{SA} at double and triple frustration to have the resulting flat dispersion associated with the stabilizer term. Achieving a junction with E_J and $E_C \sim 4$ K with Al electrodes is not possible due to the small superconducting gap of Al and the electronic capacitance that arises when the junction plasma frequency approaches the superconducting gap frequency [71]. Thus, future protected qubits incorporating this stabilizer mechanism will need to utilize small-area junctions fabricated from a larger gap superconductor such as granular aluminum. If we achieve these parameters and assume 1/f magnetic flux noise with an amplitude of 1 $\mu \Phi_0/\sqrt{\text{Hz}}$ at 1 Hz [72, 73], we estimate that we could achieve a T_2 on the order of 1 ms at frustration.

We will also need to reduce the rate of quasiparticle poisoning on the device, so that the quasiparticle poisoning timescale is at least minutes, since any QP poisoning of the intermediate islands is fatal. A more compact shunt capacitor will also bring the spurious antenna modes of the device to higher frequencies. This will prevent lower frequency external radiation from coupling to the antenna modes and generating QPs at the plaquette junctions. A smaller shunt is also important for reducing the charge sensing area and the rate of offset charge jumps on the logical island due to high energy particle impacts. Another benefit of a more compact shunt will be to help to reduce the spurious excitation of the qubit to higher levels. We can also implement more engineering of the superconducting gaps of the device to create regions where quasiparticles trap away from the plaquette junctions and intermediate islands. On a sample with more traditional transmon qubits measured on the same fridge as this device, we were able to achieve times between quasiparticle poisoning events approaching 1 minute [74]. This can potentially get pushed longer with gap engineering and even better thermalization of the device.

8.3 Protected gates with charge-parity qubits



Figure 8.1: Schematic of a protected qubit with shunt capacitor and superinductor, with connections to the logical island that are able to be modulated. Break in line symbolizes the SQUID switch that couples the shunt capacitor and the shunt superinductor to the logical island. The SQUID switch to the shunt capacitor will be normally closed, but will be opened briefly during X gates (in phase basis); the SQUID switch to the shunt superinductor will be normally opened, but will be closed briefly during Z gates (in phase basis).

The SQUID switches between the plaquette chain and the shunt capacitor and shunt superinductor will be used to perform gates on the qubit (Fig. 8.1). When the SQUID switch is frustrated (opened) for a brief duration, the effective charging energy of the logical island increases, causing a differential evolution of phase between the even and odd charge states. This corresponds to tunneling between the 0 and π wells. This allows the qubit state to oscillate between 0 and π which can be used to implement an X gate in the phase basis. To perform a Z gate, we will need to shunt the plaquette chain with a superinductor. Closing the second SQUID switch for a brief duration so that the superinductor shunts the plaquette chain will allow the different parity states to accumulate a relative phase, which is what is needed to implement a Z gate in the phase basis.

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