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Amplifier Architectures for Wireless Communication Systems

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ABSTRACT

Ever-increasing demand in modern wireless communication systems leads researchers to focus on design challenges on one of the main components of RF transmitters and receivers, namely amplifiers. On the transmitter side, enhanced efficiency and broader bandwidth over single and multiple bands on power amplifiers will help to have superior performance in communication systems. On the other hand, for the receiver side, having low noise and high gain will be necessary to ensure good quality transmission over such systems. In light of these considerations, a unique approach in design methodologies are studied with low noise amplifiers (LNAs) for RF receivers and the Doherty technique is analyzed for efficiency enhancement for power amplifiers (PA) on the transmitters. This work can be outlined in two parts.

In the first part, Low Noise RF amplifier designs with Bipolar Junction Transistor (BJT) are studied to achieve better performing LNAs for receivers. The aim is to obtain a low noise figure while optimizing the bandwidth and achieving a maximum available gain. There are two designs that are operating at different center frequencies and utilizing different transistors. The first design is a wideband low-noise amplifier operating at 2 GHz with a high power BJT. The proposed design uses only distributed elements to realize the input and output matching networks. Additionally, a passive DC bias network is used instead of active DC bias network to avoid possible complication due to the lumped elements parasitic effects. The matching networks are designed based on the reflection coefficients that are derived based on the transistor's available regions. The second design is a low voltage standing wave ratio (VSWR) amplifier with a low noise figure operating at 3 GHz. This design is following the same method as in the first design. Both these amplifiers are designed to operate in broadband applications and can be good candidates for base stations.

The second part of this work focuses on the transmitter side of communication systems. For this part, Doherty Power Amplifier (DPA) is analyzed as an efficiency enhancement technique for PAs. A modified architecture is proposed to have wider bandwidth and higher efficiency. In the proposed design, the quarter-wave impedance inverter was eliminated. The input and the output of the main and peak amplifiers are matched to the load directly. Additionally, the input and output matching networks are realized only using distributed elements. The selected transistor for this design is a 10 W Gallium Nitride (GaN). The fabricated amplifier operates at the center frequency of 2 GHz and provides 40% fractional bandwidth, 54% of maximum power-added efficiency, and 12.5 dB or better small-signal gain. The design is showing promising results to be a good candidate for better-performing transmitters over the L- and S- band.

AMPLIFIER ARCHITECTURES FOR WIRELESS COMMUNICATION SYSTEMS

By

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DISSERTATION

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Dedicated to my beloved family.

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CHAPTER 1
INTRODUCTION

1.1 Background Information

Wireless communication has been advancing exponentially in terms of data usage over the past two decades and it has become integral to daily life with the usage of computers, smartphones, tablets, and other wireless devices. According to the Cisco Visual Networking Index [1], the global mobile data traffic has expanded 17-fold between 2012-2017. Figure 1.1 shows the forecast of the data usage by year. It is expected that the data usage will be 77 exabytes per month by 2022 which account for 20 percent of the total internet protocol (IP) traffic.

This ever-increasing demand for wireless communication requires the frequency spectrum to be utilized efficiently to accommodate high data-rate transmission. Systems that require high data-rate, such as Wireless Fidelity (Wi-Fi), Wireless Local Area Network (WLAN), Long Term Evolution (LTE), and Universal Mobile Telecommunication System (UMTS) use complex modulation schemes. These schemes result in signals with high peak-to-average power ratios (PAPR) and wide bandwidth. Therefore, transmitters for such systems necessitate power amplifiers (PA) with high efficiency, wide bandwidth, good linearity, and high output power. Power amplifiers are the key component of wireless commu-

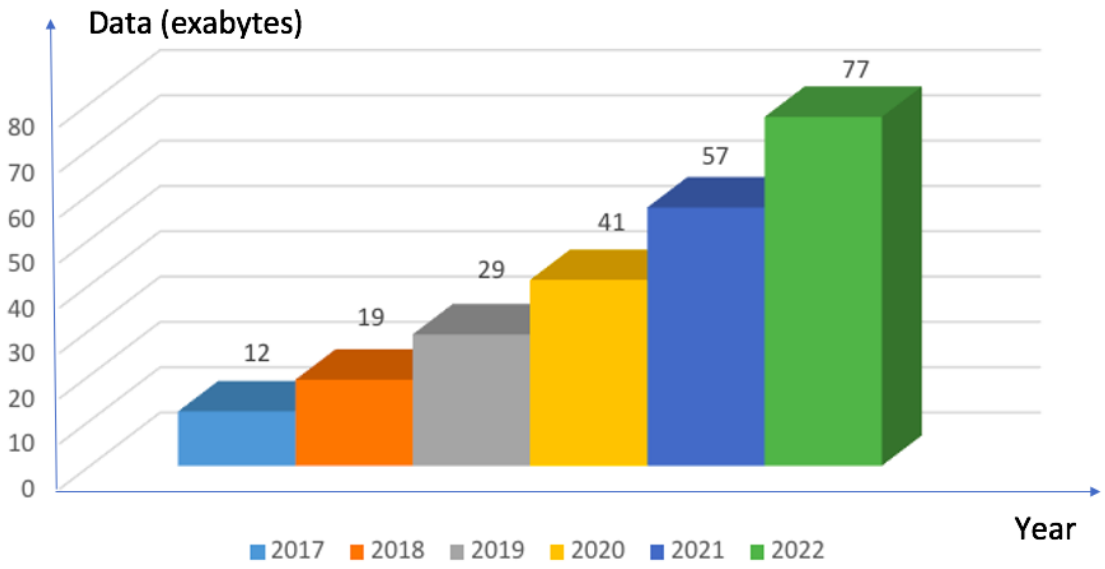


Fig. 1.1: Mobile network traffic growth and data usage per month [1].

nication systems. A power amplifier is simply defined as a device that converts DC power into the desired RF energy level with maximum efficiency [2–9].

On the other hand, receiver modules need a low noise amplifier (LNA) to receive modulated Radio Frequency (RF) signals. These low noise amplifiers should provide a low noise figure, good linearity, and high gain to provide better performance [10–15]. Low noise amplifiers are the main elements of the receiving part of the communication systems. Basically, they receive low voltage and low power signals in the RF input and then they amplify these signals without reducing the signal to noise ratio.

Figure 1.2 shows the block diagram of the RF wireless communication system. A generic RF wireless communication system consists of the following components: antenna, duplexer, communication channel, transmitter, and receiver. In this system, an antenna is a device that converts an RF signal into an electromagnetic wave in the atmosphere. Duplexer ensures bi-directional communication between antenna and transceiver (TRANSmitter and reCEIVER). It separates the transmitter from the receiver while allowing them to communicate with the same antenna. The transmitter and receiver are the components that send and receive signals between the antenna and communication channel.

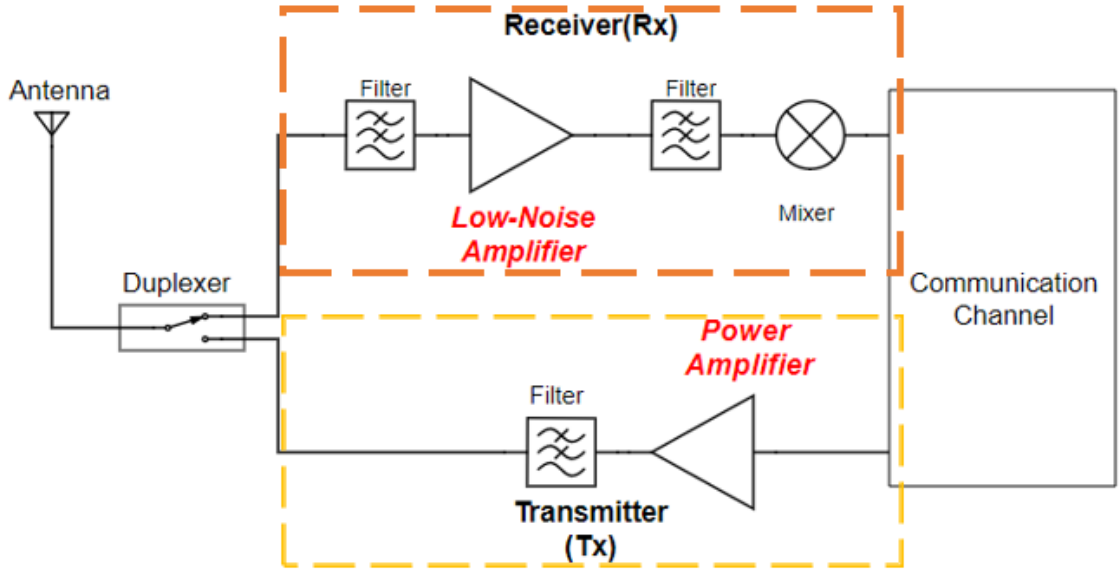


Fig. 1.2: Block diagram of RF wireless communication system.

Having a major role in the communication systems, designing LNA and PA require to focus on several key parameters. For instance, parameters for LNA design are low noise figure, high power gain, and stability. Moreover, PA design parameters are linearity, PAPR, output power, bandwidth, and efficiency. Another design parameter to consider is power consumption. Reduced power consumption can decrease design complexity caused by the need to remove heat which in turn impacts the cost and the size of the heat sink. Therefore, designing low-noise, high gain, and wideband LNA for receivers and cost-effective and energy-efficient PA for transmitters should be a priority for such systems.

Low noise and high gain are not an easy task to achieve when designing an LNA. Researchers have been implementing different topologies and methodologies for years to have a successful design. Some designs are employing lumped elements such as resistors, inductors, and capacitors. Some others utilize microstrip technology to design better performing LNA of the receiver front-end [16–20]. The main design challenges for LNA are narrow bandwidth, high noise figure, and low gain.

On the transmitter side, there are several methods to improve the efficiency of PAs at the back-off power level. However, in this work, only four of them will be introduced. These

methods are Envelope Elimination and Restoration (EER) [21], Envelope Tracking (ET) [3, 22], Outphasing [23], and the Doherty technique [24]. Each method has its advantages and disadvantages. The first three methods will be briefly covered in section 2.4. The Doherty Technique will be explained in detail because it is essential to the study undertaken. The Doherty Power Amplifier (DPA) was proposed by W.H. Doherty in 1936 and it is still one of the most popular enhancement techniques as it has a straightforward architecture and provides high efficiency with good linearity. However, bandwidth limitation is one of the drawbacks of the DPAs. This limitation is mainly caused by quarter wavelength transmission lines used to combine the output matching networks of the main and peak amplifiers. Over the years researchers and engineers have worked on a wide variety of solutions to overcome the limitations of designs.

1.2 Aim and Objectives

The frequency spectrum is over-utilized in L- and S-band (0.5-4 GHz) and there is no way to make room for an extra band in the spectrum. The increasing demand in the wireless communication system requires to have wideband, energy-efficient, and linear devices. A possible solution here is to optimize the communication system components. These components such as amplifiers are under the spotlight for researchers since they are one of the key components in RF microwave wireless communication systems.

The main focus here is to overcome design challenges on the transceiver to improve efficiency while increasing bandwidth. Thus, new schemes and topologies are under investigation.

This dissertation proposes a method to improve the performance of LNA and PA architectures for receiver and transmitter. The objectives of this study are to analyze amplifier topologies, to improve the design process and to optimize simulation to achieve better performing amplifiers.

The first part of this study focuses on LNAs which are the active devices at the front-end of the receiver. Therefore, the design process needs attention as the noise figure of the LNA affects its performance significantly. There is a trade-off between gain and the noise figure while keeping the device at a stable level. Thus, the LNA design and optimization is a challenging task to perform. For the first part of this study, two BJT-LNAs were designed, fabricated, and tested. Both designs provide good results and might be a good candidate to be used in the base stations.

The first design operates between 1.7 - 2.3 GHz. The design approach is to define optimum input and output reflection coefficients to achieve maximum unilateral transducer gain. These coefficients are calculated for both the input matching network (IMN) and the output matching network (OMN). Both networks are realized using distributed elements (symmetrical open circuit stubs). An active DC bias network is designed but not utilized in this design. Instead, a passive DC bias network is used to prevent design complexity. The design is optimized using a computer-aided design (CAD) tool to achieve the desired performance such as low noise figure, high power gain, stability, and wide bandwidth.

The second design is wideband and low VSWR LNA operating between 2.7 - 3.3 GHz. This design also applies the same strategy as in the first design but utilizes a different transistor. The selected transistor for this design is unilateral. Therefore, reflection coefficients for IMN and OMN are selected from the transistor's unconditionally stable region. Then, the maximum transducer gain is calculated based on the transistor's characteristic parameters. IMN and OMN networks are designed utilizing distributed elements. Circuit and EM simulations along with optimizations are carried out using available CAD tools. Measured results are in good agreement with EM simulation results. In both designs, lumped elements are not utilized to have simple architecture and reliable performance.

The classical PA architectures suffer from low efficiency and high-power consumption. Therefore, improvement of efficiency is a necessary step when designing PA.

The second part of this study focuses on the efficiency enhancement of PAs. The Do-

herty technique was selected to investigate and implement for this purpose. Design considerations are bandwidth, overall efficiency, and high peak-to-average power ratio (PAPR).

The proposed design for this part is a wideband symmetrical DPA operating between 1.7-2.3 GHz. Design theory is based on the elimination of a quarter wavelength transmission line at the combiner section to achieve wider bandwidth. Main and peak amplifiers are using a 10 W GaN transistor from Cree. The design provides 54% power-added efficiency with 40% fractional bandwidth. Measured results validate the design methodology.

1.3 The Structure of the Dissertation

In this research, the main focus is to improve efficiency while increasing bandwidth on the amplifiers for modern communication systems. To achieve this goal, design techniques are analyzed and implemented on LNA and PA. In the first part of this study, low noise amplifiers for broadband wireless applications are designed and fabricated on the different frequency bands. Both designs are using BJT transistors. In the second part, the Doherty efficiency technique for power amplifiers is studied. Wideband and energy-efficient DPA is designed using a 10 W GaN transistor.

In chapter 2, the fundamental theory and design process about microwave transistor amplifiers are presented. Moreover, the classical theory of RF power amplifier, classes of operation, and efficiency enhancement techniques are introduced. Furthermore, the transistor technologies are compared and the choice of transistor selection for the PA design is explained.

In chapter 3 and 4, two low noise amplifier designs for the receiver section of communication systems are presented. The first design is a wideband low-noise amplifier operating at the center frequency of 2 GHz [25]. The second design is a wideband and low VSWR amplifier working at the center frequency of 3 GHz [26]. Both amplifiers are designed, fabricated, and tested. Another LNA design with different transistor is design, fabricated,

tested and also published by the author, however, it was not included in this thesis [27].

In chapter 5, an extensive literature review on single and dual-band DPA is presented. Additionally, single-stage wideband DPA design methodology utilizing GaN transistor is explained and experimental results are provided. The design operates at the center frequency of 2 GHz and eliminates the quarter wavelength impedance inverter to achieve wider bandwidth.

In chapter 6, the conclusions of this study, contributions, as well as the future research ideas are discussed.

1.4 List of Publications

The following list consists of publications from the work carried out during the graduate studies at Syracuse University.

Published

- M. O. Kok, F. Kaburcuk, and E. Arvas, "A wideband lna at 2 ghz," 30th International Review of Progress in Applied Computational Electromagnetics Society (ACES) , Jacksonville, Florida, United States Of America, pp.505 - 509, 2014.

- M. O. Kok, B. J. Martinez, V. Sanandiya, and E. Arvas, "Microwave transistor amplifier design procedure" 30th International Review of Progress in Applied Computational Electromagnetics Society (ACES), Jacksonville, Florida, United States Of America, pp.664 - 668, 2014.

- F. Kaburcuk, M. O. Kok, and E. Arvas, "Design of low noise amplifier at 2 ghz," 30th International Review of Progress in Applied Computational Electromagnetics Society (ACES), Jacksonville, Florida, United States Of America, pp.675-678, 2014.

- F. Kaburcuk and M. O. Kok, "Fast wideband solution using MBPE with MOM," 2017 International Applied Computational Electromagnetics Society Symposium -

Italy (ACES), Florence, 2017, pp. 1-2, doi: 10.23919/ROPACES.2017.7916377.

- G. Kalinay, F. Kaburcuk and M. O. Kok, "A microwave bandpass filter design," International Symposium on Applied Sciences and Engineering (ISASE-2018) , Erzurum, Turkey, pp.137-139, 2018.

In preparation

- M. O. Kok, F. Kaburcuk, and Q. W. Song, "A modified Doherty-like amplifier design with a 10 w gan transistor", Journal paper.
- M. O. Kok, F. Kaburcuk, P. Aaen, and Q. W. Song, "Advancements on broadband and multiband Doherty power amplifier designs using gan transistors", Review paper.

CHAPTER 2
RF-MICROWAVE AMPLIFIER OVERVIEW

This chapter presents an overview of RF-Microwave amplifiers. This study focuses on the improvement of the receiver and transmitter. Therefore, knowing the theory behind these components has great importance. The first section discusses the single-stage transistor amplifier design theory, specifically on LNA whereas the second section provides fundamentals on RF PA as well as information about classes of operation. The third section explains performance parameters for both LNA and PA. Forth section introduces efficiency enhancement techniques for PA such as Envelope Elimination and Restoration (EER), Envelope Tracking (ET), Outphasing (Chireix), and the Doherty. The Doherty technique will be analyzed in more detail in comparison with other methods and this will lay the foundation for chapter 5. The last section of this chapter focuses on transistor technologies and gives insight into the device of choice for PA design in this research.

2.1 Low-Noise Amplifier

This section gives insight into microwave transistor amplifier theory and LNA design for the receiver part of the wireless communication systems. First, brief information about transistors will be provided. Then, the basic formulations for the microwave transistor amplifier design procedure will be explained.

Transistors were invented in 1947 by three engineers at Bell Lab. They are semiconductor devices with at least three terminals for connections and are used for amplifying and rectifying electronic signals.

The transistor is one of the main components of the electronic circuits and they might be classified as junction transistors or field-effect transistors (FET). Junction transistors can be considered in two categories, bipolar junction transistor (BJT) and heterojunction bipolar transistor (HBT) [10,11,15,16]. There are also two types of commercially available BJTs: n-type and p-type which are shown in figure 2.1. The frequency range for the silicon junction transistors is between 2-10 GHz for amplifiers and up to 20 GHz for oscillators. Therefore, BJTs are a good alternative to devices operating over L- and S-band.

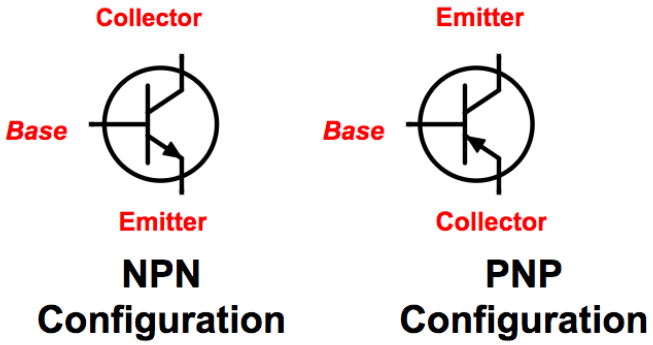


Fig. 2.1: The bipolar junction transistor types.

BJTs are low cost and high-performance devices that are made of silicon (Si) and commonly used in low noise amplifiers [28–30]. For these reasons, BJT is selected for LNA designs in this chapter.

The design of microwave transistor amplifiers has been studied by researches for years

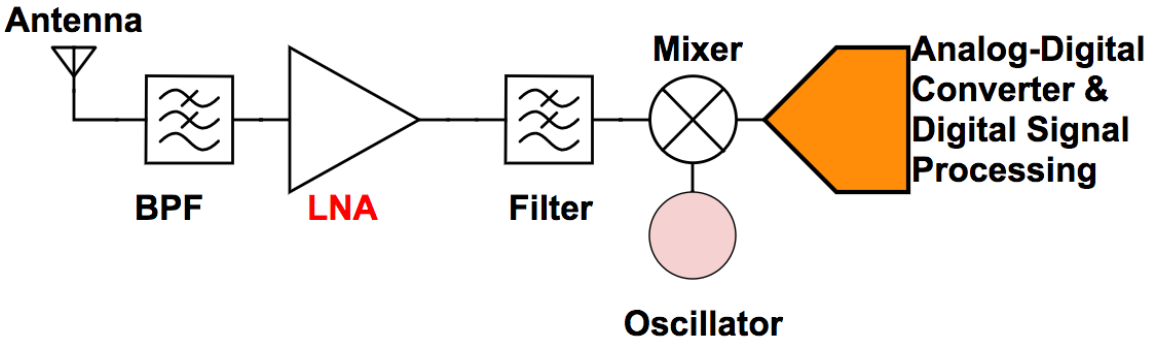


Fig. 2.2: Front-end receiver circuit schematic.

[17–20, 31–36]. Among these amplifiers, LNAs are one of the most important components of the front-end of the receivers as seen in figure 2.2. The function of the LNA in the system is to increase the gain while keeping the noise as low as possible. Noise should be kept at the minimum so that the device might capture low power and low voltage signal. Another parameter that needs to be taken into account in the design process is input and output VSWR as it shows how well the input and output circuits are matched. Therefore, the design methodology and procedure are highly sensitive and requires delicate attention.

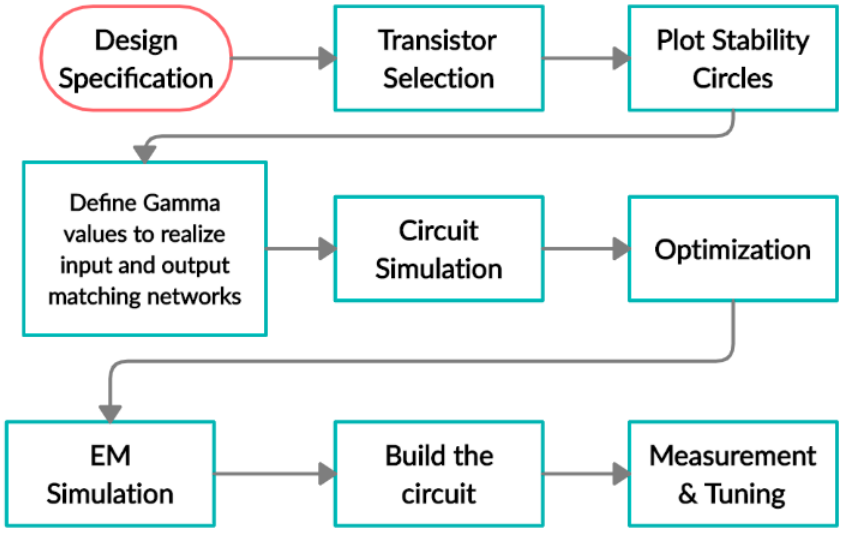


Fig. 2.3: Low noise amplifier design flow chart.

Figure 2.3 shows the design flow chart for microwave transistor amplifiers. Fundamentals of microwave transistor amplifiers should be studied and well-analyzed to develop a

methodology and a step by step procedure for the design.

The process starts with defining the specifications that the amplifier is expected to provide. Then, the transistor selection comes next. Transistor choice is important. Scattering parameters (S-parameters of the transistor), which describe the electrical behavior of the network, indicate the maximum achievable power gain for a given bias condition. Also, the datasheet of the possible transistors should be reviewed since it contains parameters such as noise figure, breakdown voltage, and DC current, etc.

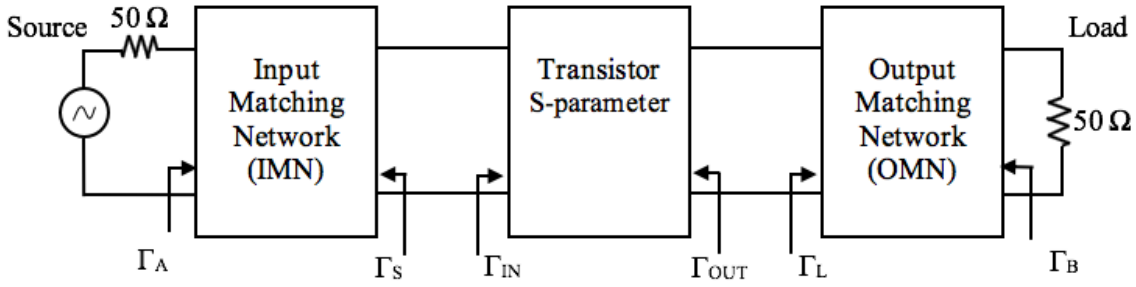


Fig. 2.4: Microwave transistor amplifier block diagram.

After the transistor is selected, S-parameters can be used to determine power gain, stability, and reflection coefficients. Mathematical formulations that will be provided in this chapter are from the literature [10–14]. Figure 2.4 shows the basic block diagram of the microwave transistor amplifier. Here, input and output reflection coefficients of the transistor are given as following.

$$\Gamma_{IN} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \tag{2.1}$$

$$\Gamma_{OUT} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \tag{2.2}$$

where Γ_S and Γ_L are reflection coefficients for the source and the load. Here, S_{11}, S_{12}, S_{21}, and S_{22} are the S-parameters of the two port device (transistor) and they represent, input port voltage reflection coefficient, reverse voltage gain, forward voltage gain, and output port voltage reflection coefficient.

There are three different definitions for the gain of the overall network based on the power used such as the available power gain G_A, the power gain G_P, and the transducer power gain G_T. The set of formulations for these expressions is given in equations 2.3, 2.4, and 2.5.

$$G_A = \frac{P_{AVN}}{P_{AVS}} = \frac{1 - |\Gamma_S|^2}{|1 - S_{11}\Gamma_S|^2} |S_{21}|^2 \frac{1}{1 - |\Gamma_{OUT}|^2} \tag{2.3}$$

where P_{AVN} is the available power from the network and P_{AVS} is the available power from the source.

$$G_P = \frac{P_L}{P_{IN}} = \frac{1}{1 - |\Gamma_{IN}|^2} |S_{21}|^2 \frac{1 - |\Gamma_L|^2}{|1 - S_{22}\Gamma_L|^2} \tag{2.4}$$

where P_L is the power delivered to the load and P_{IN} is the power input to the network.

$$G_T = \frac{P_L}{P_{AVS}} = \frac{1 - |\Gamma_S|^2}{|1 - \Gamma_{IN}\Gamma_S|^2} |S_{21}|^2 \frac{1 - |\Gamma_L|^2}{|1 - S_{22}\Gamma_L|^2} \tag{2.5}$$

Stability is another parameter that shows that the amplifier operates on a stable level without going into oscillation. In this case, oscillation means the transistor might cause negative feedback at the input and output of the amplifier. In an amplifier, oscillation occurs if magnitude of S_{11} and S_{22} are greater than 1.

The selected transistor might be unconditionally stable or potentially unstable. There are two different approaches to design an amplifier in these situations. For the unconditionally stable unilateral transistor, where S_{12} = 0, stability can be determined by the input and output reflection coefficient of the overall amplifier. These are shown as Γ_A and Γ_B in figure 2.4. Both values should be less than 1 to meet this requirement. Γ_A and Γ_B are given by the following expressions.

$$|\Gamma_A| = \left| S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right| < 1 \tag{2.6}$$

$$|\Gamma_B| = \left| S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \right| < 1 \tag{2.7}$$

The input and output stability circles of the transistor should be plotted to define the available regions on the Smith chart. Then from these available regions, reflection coefficients of the input and output matching networks, Γ_S and Γ_L, need to be chosen. Stability circle formulations for the radius values of Γ_S and Γ_L are expressed by:

$$r_S = \left| \frac{S_{12}S_{21}}{|S_{11}|^2 - |\Delta|^2} \right| \tag{2.8}$$

and

$$r_L = \left| \frac{S_{12}S_{21}}{|S_{22}|^2 - |\Delta|^2} \right| \tag{2.9}$$

where $\Delta = S_{11}S_{22} - S_{12}S_{21}$.

DC bias network design helps smooth transmission and ensures the desired performance. Detailed information regarding bias network design can be found in the literature [10, 11, 13].

Once the design process of IMN and OMN is completed, circuit simulations can be performed. If the initial performance is not at the desired level, optimization tools from the computer-aided design software can be utilized. Once the circuit simulations are finalized, the design needs to be run in EM simulation as this gives closer results to the actual measurement performance. The last step is to fabricate the circuit and complete the measurements of the amplifier. If necessary, the fabricated circuit can be tuned to achieve the desired outcomes. It might take several iterations for simulations and several fabrications to produce the optimum design.

The design approach and the process of a microwave transistor amplifier based on defining the transducer gain and stability circles of an unconditionally stable transistor are explained in this section. Additionally, there are different approaches to design a transistor

amplifier using constant gain circles, and constant VSWR circles, however, they will not be used in this study. Wideband BJT amplifier designs with different model transistors are presented in the following chapters. Both designs have different operating frequencies and bandwidths.

2.2 Power Amplifier

The wireless communication system has undergone important developments over the last decade and all of these developments require or call for the transformation of the existing structures. Especially, the number of wireless devices has increased exponentially and it is projected that this growth will continue in the upcoming years [1]. This increase will bring higher data usage, the need for wider bandwidth and more energy consumption. Eventually, all these outcomes will require to design a better-performing power amplifier in the front-end of the transmitter.

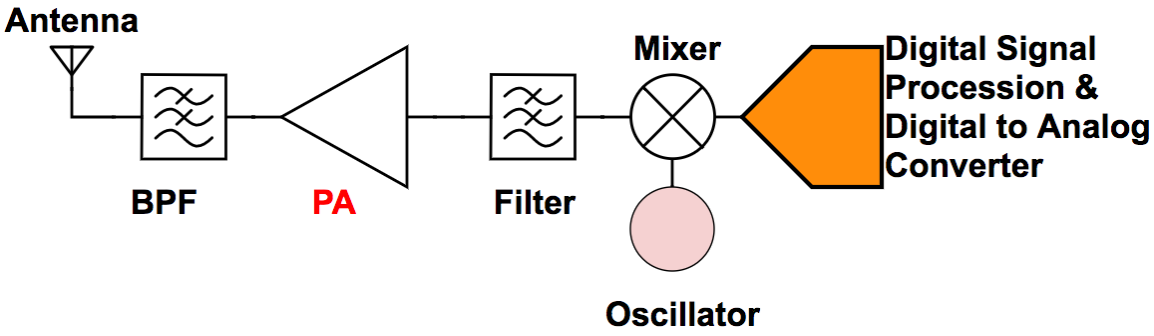


Fig. 2.5: Front-end transmitter circuit schematic.

The power amplifier is a device that converts DC power into the desired RF energy level and is an important part of the transmitter which is one of the main sections of communication system. Figure 2.5 shows a front-end transmitter circuit schematic.

Figure 2.6 shows the design flow chart of a conventional PA. It is slightly different from the LNA flow chart that is explained in section 2.1. In PA design, optimum impedance to match the input and output matching networks is determined by load / source pull simula-

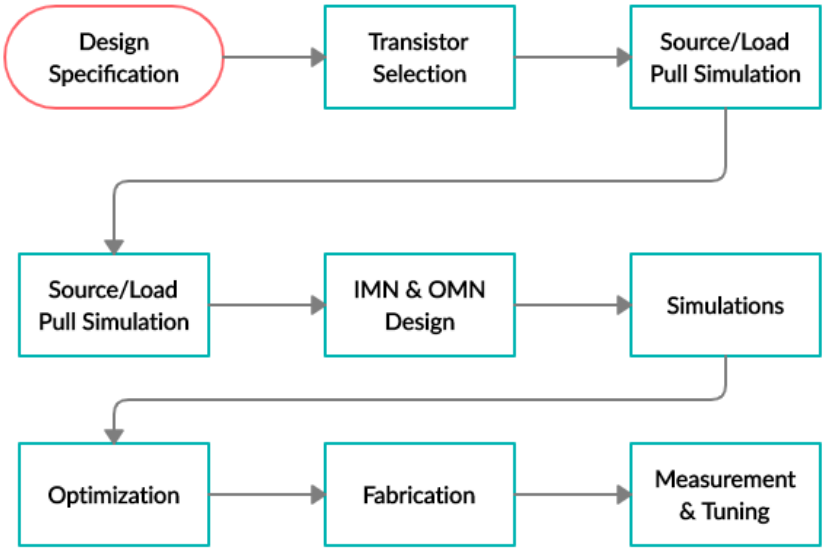


Fig. 2.6: Power amplifier design flow chart.

tion using the transistor's model provided by the vendor. Details about load / source pull simulation will be explained in section 5.2. The rest of the steps are similar to the LNA design procedure and introduced in section 2.1. So, it will not be repeated in this section.

2.2.1 Classes of Operation

Power amplifiers can be analyzed in two groups based on the operation mode such as current waveform mode and switch mode. The current waveform mode operating amplifiers are divided into classes depending on their conduction angle and DC bias condition. These are class A, AB, B, and C [4, 5]. Figure 2.7 presents the waveform comparison of different classes with respect to the conduction angle [37]. Switch mode amplifiers such as class D, E, and F operates as a switch because the transistor is either on or off.

Conventional PAs are classified by the conduction angle which is the period when the transistor carries current. In the current waveform mode, the input signal is a sinusoidal wave and the output signal is a linear reflection of the input signal. The mathematical expression of an input signal voltage is given in the following:

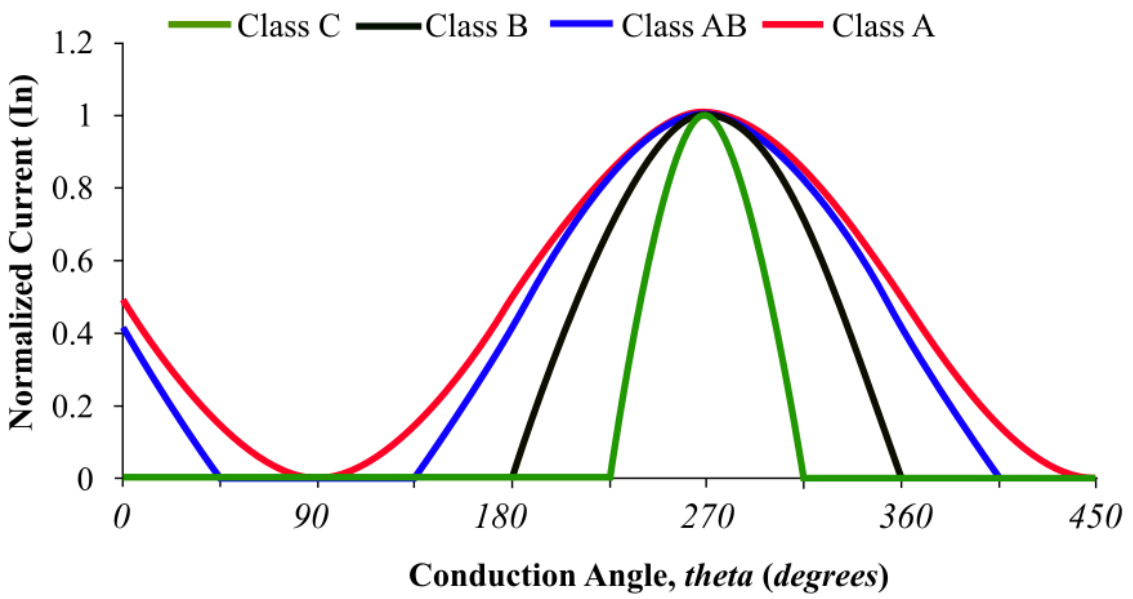


Fig. 2.7: Class of operation waveform comparison respect to conduction angle.

$$V_{in} = V_q + V_{swing}(cos\theta) \tag{2.10}$$

Here, V_q is the quiescent voltage of a transistor when there is no signal applied and V_{swing} is the voltage swing, which defines a range for the input voltage. Drain current i_d of the current waveform modes is represented by the following expressions.

$$i_d = \begin{cases} I_q + I_{pk}cos(\theta) & -\alpha/2 \leq \theta \leq \alpha/2 \\ 0 & \pi < \theta < -\alpha/2; \alpha/2 < \theta < \pi \end{cases} \tag{2.11}$$

Where as the drain voltage is defined as:

$$V_d = V_{DC} - i_d Z_L = V_{DC} - I_1 R_L cos(\theta) = V_{DC} - V_{swing}cos(\theta) \tag{2.12}$$

Here, V_{DC} is the voltage that is applied to the transistor where as Z_L is the impedance seen by the transistor and R_L is the load.

The following subsections cover the current waveform operating classes A, AB, B, and C as they are the ones utilized in DPAs in the following chapter

In the class A amplifier, the bias point is selected from the active region of the transistor that is in the middle of the load line where the DC current is constant. Since the transistor is on for the full cycle of the signal, the conduction angle is 360^o (2π). Figure 2.8 and Figure 2.9 represent the class A amplifier voltage and current waveform with respect to the conduction angle [8].

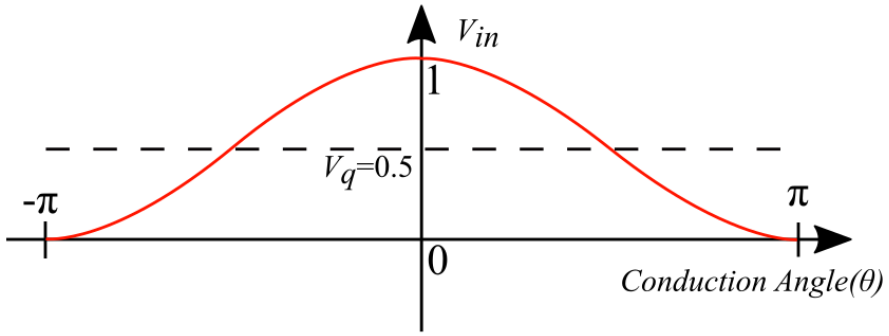


Fig. 2.8: Class A amplifier voltage waveform.

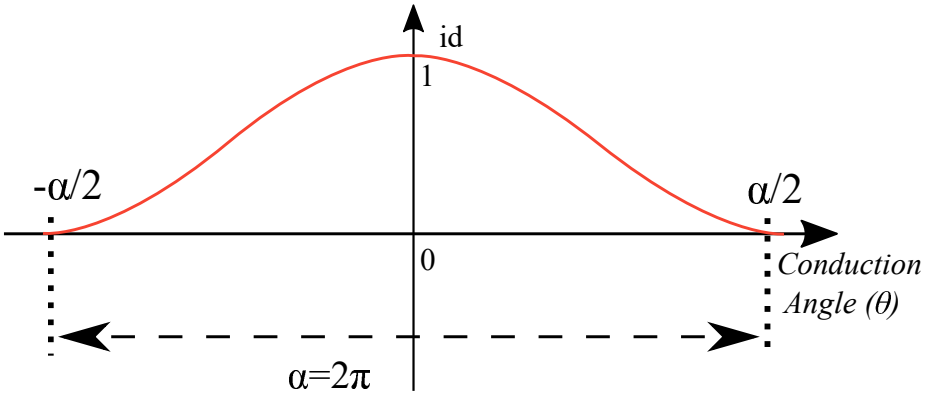


Fig. 2.9: Class A amplifier current waveform.

The transistor is active all the time. Therefore, it has high linearity and low distortion. However, efficiency is low because the device continuously draws current. The theoretical efficiency of class A amplifier can be derived from the following expressions [38].

$$\eta = \frac{P_{out}}{P_{DC}} \tag{2.13}$$

where P_{DC} is the DC power consumption and given by:

$$P_{DC} = V_{DC} I_{DC} \tag{2.14}$$

The maximum output power is given by:

$$P_{out} = \frac{1}{2} V_{DC} I_{DC} \tag{2.15}$$

Thus, the efficiency is given by:

$$\eta = \frac{1}{2} \tag{2.16}$$

Therefore, the efficiency of the class A amplifier is 50% in an ideal case and it's expected that it might be lower in practical application. This is a major disadvantage for power amplifiers as they are known for high power-consuming devices. Thus, the class A amplifier is a good candidate for systems that require high linearity and low power.

The class B amplifier is biased at transistor's cut-off voltage. Therefore, the transistor is active only positive or negative half of the input cycle at any given time. Thus, the conduction angle is 180^o (π).

Figure 2.10 and Figure 2.11 show the class B amplifier voltage and current waveform with respect to conduction angle [8].

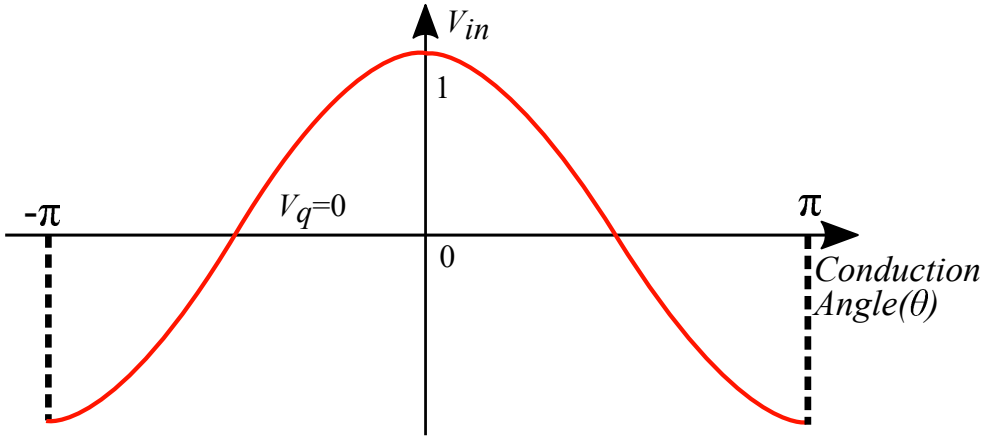


Fig. 2.10: Class B amplifier voltage waveform.

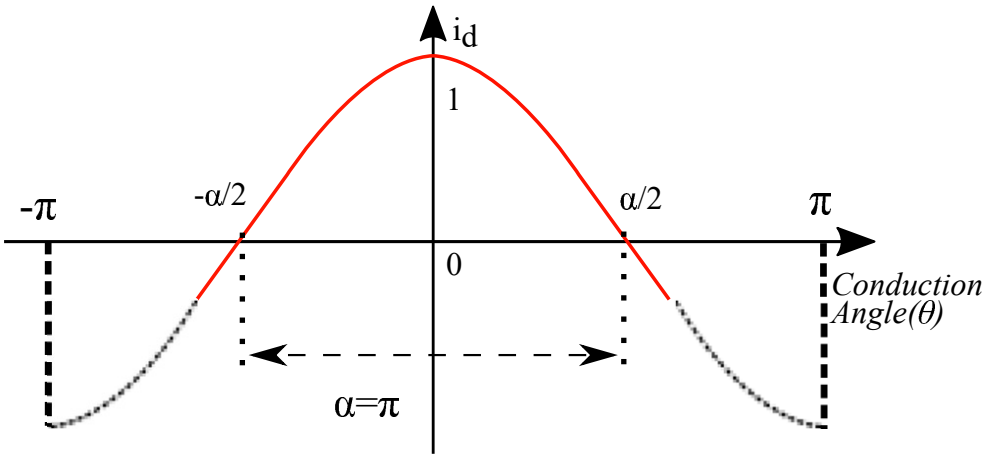


Fig. 2.11: Class B amplifier current waveform.

The class B bias is an ideal candidate for push-pull amplifiers in which there are two transistors in the topology. The first transistor conducts during the positive input cycle, while the second transistor conducts the negative input cycle. The efficiency of the class B amplifier is given by the following equations;

$$\eta = \frac{P_{out}}{P_{DC}} \tag{2.17}$$

$$P_{DC} = V_{DC}\frac{I_{max}}{\pi} \tag{2.18}$$

$$P_{out} = \frac{1}{2}V_{DC}\frac{I_{max}}{2} \tag{2.19}$$

Thus, the efficiency is given by:

$$\eta = \frac{\pi}{4} \tag{2.20}$$

Therefore, the theoretical efficiency of the class B amplifier is equal to 78.5%. Even though the class B provides better efficiency than the class A, its linearity is worse due to intermodulation distortion products.

Class AB amplifier has similar linearity performance as class A with better theoretical efficiency.

In the class AB configuration, transistor's bias point is chosen between the class A and the class B which is a little higher than the cut-off voltage of the transistor. Therefore, the conduction angle is between 180^o (π) and 360^o (2π). In this case, transistor would conduct more than half the input cycle but less than the full input cycle [39]. Figure 2.12 and Figure 2.13 show the class AB amplifier voltage and current waveform with respect to the conduction angle [8]. In terms of linearity, the class AB provides higher performance than the class B but lower than the class A. On the other hand, the class AB has higher efficiency than the class A because transistor is on for more than half the input cycle.

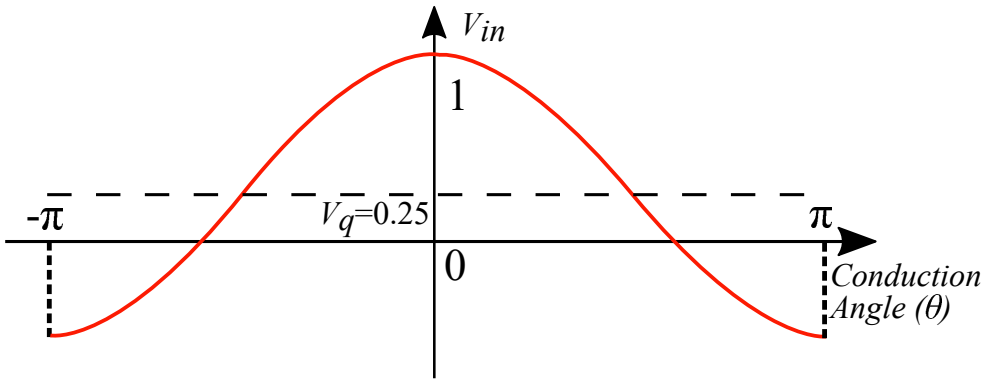


Fig. 2.12: Class AB amplifier voltage waveform.

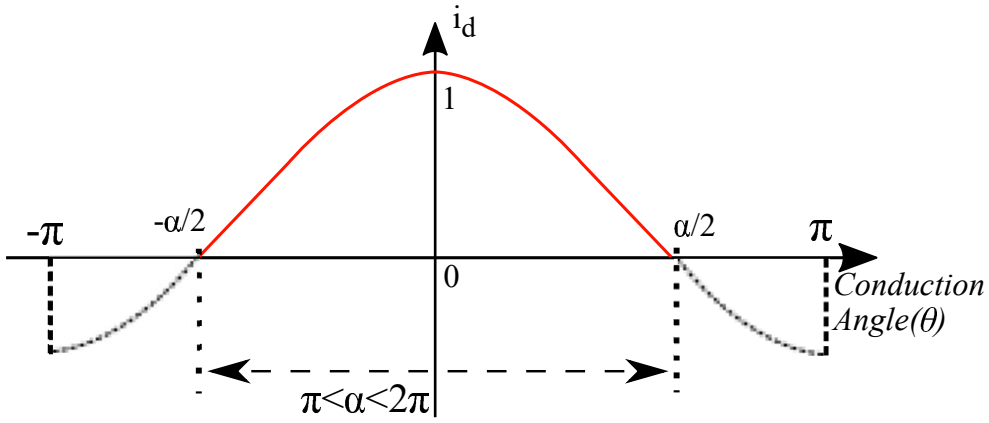


Fig. 2.13: Class AB amplifier current waveform.

Theoretical efficiency for the class AB amplifier is between 50% and 78.5%. There is a

good trade-off between linearity and efficiency in the class AB operation mode. Therefore, it is a preferred class of operation in practice. Also, as it is covered in section 2.5, the class AB bias mode is used in the main amplifier of the Doherty amplifiers.

In the class C amplifier, the transistor is biased lower than the cut-off voltage level. Thus, the transistor is active less than half of the input cycle. In this case, the conduction angle is between 0^o and 180^o (π) which is reduced compared to class A, class B, and class AB amplifiers. This reduction in the conduction angle yields high efficiency. Figure 2.14 and Figure 2.15 show the class AB amplifier voltage and current waveform respect to the conduction angle [8].

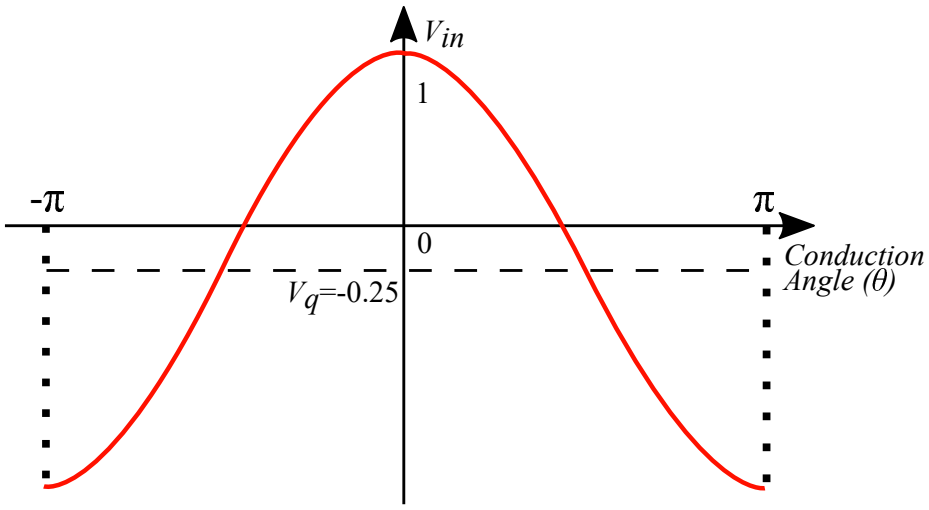


Fig. 2.14: Class C amplifier voltage waveform.

Theoretical efficiency increases to 100% as the conduction angle decreases to 0^o. In practical applications, reported class C amplifiers can reach 85% efficiency while the conduction angle is 150^o [2, 3].

Figure 2.16 shows the output power and efficiency behavior of different class amplifiers based on their conduction angle [40]. Output power goes to zero when the conduction angle decreases. On the contrary, efficiency increases with the reduction of the conduction angle. The class A and the class B have similar level of output power whereas the class AB has the highest output power.

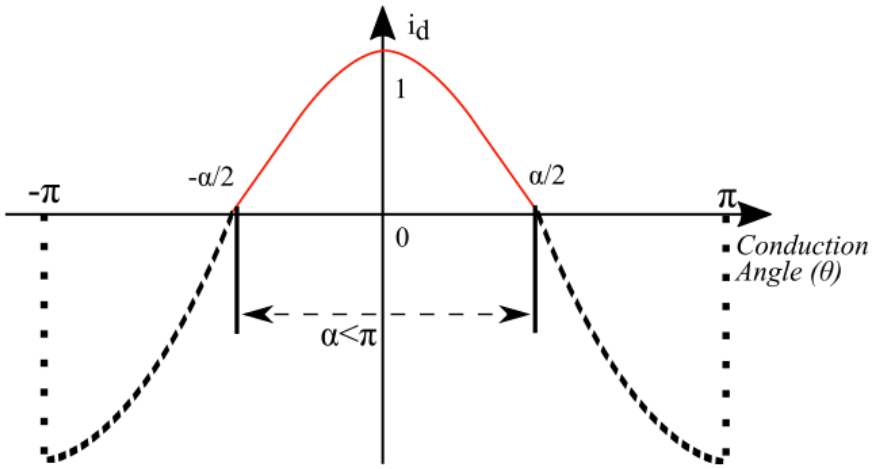


Fig. 2.15: Class C amplifier current waveform.

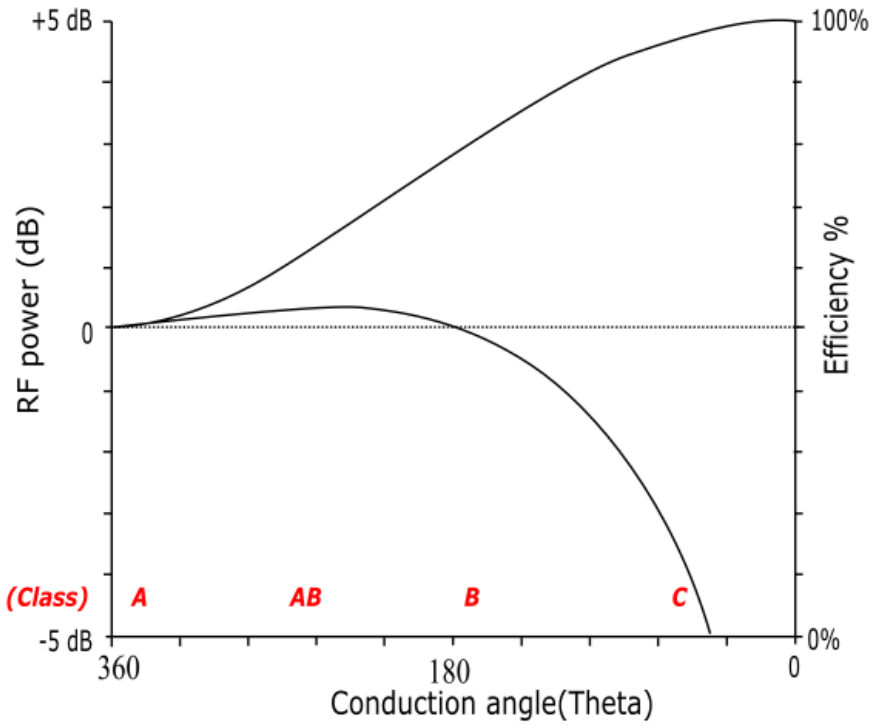


Fig. 2.16: Conduction angle, output power and efficiency performance based on class of operation.

Table 2.1 presents the performance summary for different amplifier classes. In conclusion, the class A amplifier provides high linearity with 50% efficiency while giving moderate output power. Whereas the class B gives high efficiency with moderate linearity.

Additionally, the class AB delivers good linearity, high output power and high efficiency and the class c provides high efficiency with poor linearity.

Class of Operation	**Condution Angle (θ)**	**Efficiency**	**Linearity**
A	2π	50%	High
B	π	78.50%	Moderate
AB	$\pi < \theta < 2\pi$	> 78.5%	Good
C	$0 < \theta < \pi$	100%	Low

Table 2.1: Performance summary of amplifier classes.

2.3 Amplifier Performance Parameters

The design performance of both LNA and PA depends on the measurement results. These results provide important parameters which show the characteristics of the amplifier. These characteristics are, gain, efficiency, linearity, noise figure, and PAPR. The following subsections introduce these parameters and provide mathematical expressions.

2.3.1 Gain

Gain is an important design variable for amplifiers. Even though the high gain is desirable to achieve, it is constrained with the selected transistor and design methodology. Power gain is defined as the ratio of the output power, P_{out}, to the input power, P_{in}. Here P_{out} is the power delivered to the load. Figure 2.17 shows the input and output representation of an amplifier.

$$Gain(G) = \frac{P_{out}}{P_{in}} \tag{2.21}$$

$$Gain = 10\log\left(\frac{P_{out}}{P_{in}}\right)(dB) \tag{2.22}$$

Power level is used to express gain, however, it is commonly notated in terms of decibels (dB). Therefore, Eq. 2.22 is generally used to formulate gain in dB [2, 5].

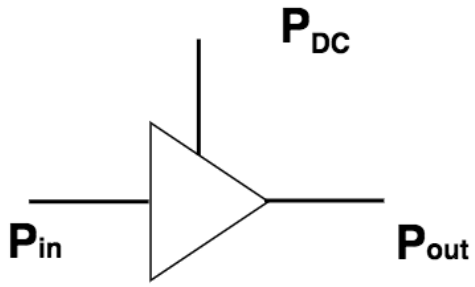


Fig. 2.17: Basic Amplifier Diagram.

2.3.2 Efficiency

Since power amplifiers are the main power-consuming components of any communication system, they should be operating efficiently to keep the heat dissipation and energy consumption as low as possible. This condition makes the efficiency one of the main parameters of power amplifier design. Mainly, efficiency can be expressed in three ways. These are drain efficiency (η), power added efficiency (PAE) and average efficiency, η_{AVG}. Drain efficiency (η) measures the power conversion of the DC input power to RF output power.

$$\eta = \frac{P_{out}}{P_{DC}} \tag{2.23}$$

where $P_{DC} = V_{DC} I_{DC}$.

Power added efficiency (PAE) is different from the drain efficiency. In PAE, gain of the power amplifier is included. Thus, the PAE formulation is given as follows:

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} = (\frac{P_{out}}{P_{DC}})(1 - \frac{1}{G}) \tag{2.24}$$

Therefore, PAE becomes;

$$PAE = \eta(1 - \frac{1}{G}) \tag{2.25}$$

Another efficiency measure is average efficiency which can be calculated at any given time with a certain output power level. Basically, average efficiency is maximum at the peak envelope power (PEP) and it is the ratio of the average output power to the average input power [2, 5].

$$\eta_{AVG} = \frac{P_{outAVG}}{P_{inAVG}} \tag{2.26}$$

In recent years, efficiency enhancement techniques have been studied extensively. There are several methods that are preferably used in many designs. This dissertation focuses on Doherty technique which will be discussed in more detail in section 2.5.

2.3.3 Linearity

The linearity of an amplifier shows that the amplified signal is transmitted without distortion for both amplitude and the phase. Distortion might lower the signal quality but the main concern here is the possibility of generating signal on the adjacent channels. Distortion is caused by the transistor that is used in the amplifier or design methodology of the circuit. On the other hand, non-linearity is caused by the distortion on the signal and can generally be seen amplitude as distortion (AM-AM) and phase distortion (AM-PM) [38, 41]. Therefore, parameters that are showing non-linearity of the amplifier such as 1-dB compression point $(P1dB)$ and intermodulation distortion (IMD) can be used to check linearity.

2.3.4 1-dB compression point

Theoretically, the output power level should be increasing linearly with respect to the input power level. However, the practical response of an amplifier shows that the output power

level reaches saturation point, (P_{sat}), when the input power level is driven to this point. 1-dB compression point, where the difference between theoretical behavior and practical behavior is 1 dB. It means amplifier gain is decreased by 1 dB at the output. After this input power level, distortion happens and the amplifier shows a non-linear response due to the nature of the transistor.

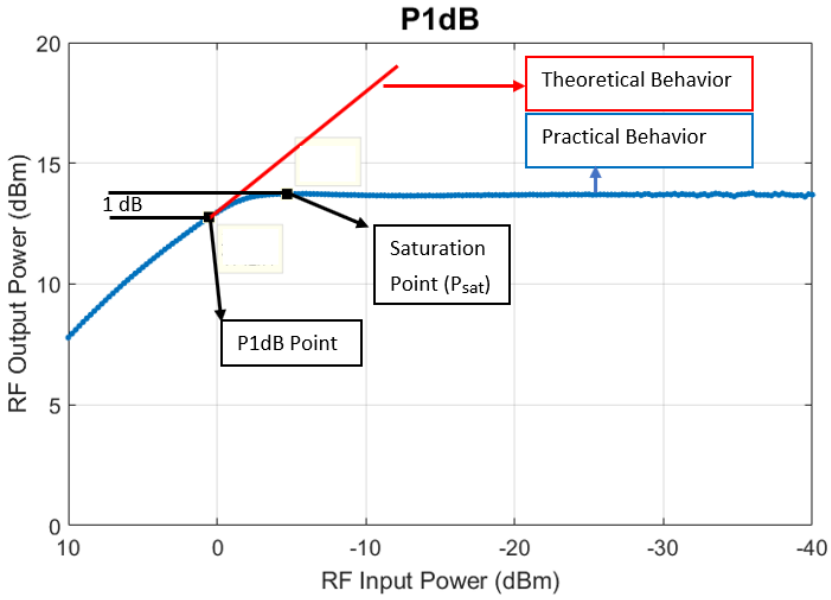


Fig. 2.18: 1-dB compression point of an amplifier.

Figure 2.18 shows the representation of the 1-dB compression point. The mathematical interpretation of P1dB is given by the following equation.

$$P_{in}(dBm) = P_{out}(dBm) + G_{1dB}(dB) \tag{2.27}$$

where G_{1dB} is the linear gain of the amplifier at the compression point.

2.3.5 Inter Modulation Distortion

Inter modulation distortion (IMD) is another parameter to check the linearity and non-linearity of an amplifier. IMD occurs when more than one signal with equal power is applied to the amplifier at the same time. Supplying multiple signals to the amplifier is

called a two-tone test. Figure 2.19 represents the frequency spectrum of a two-tone signal test of an amplifier. This test causes intermodulation products at the output of the amplifier along with the original input signals.

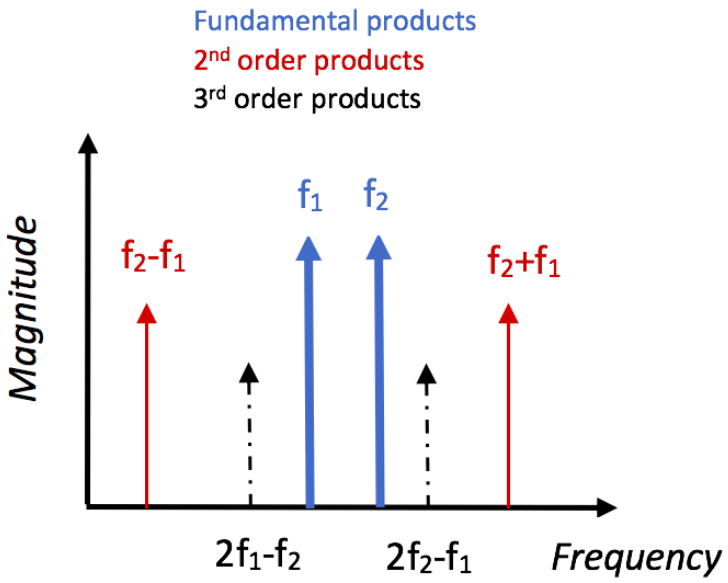


Fig. 2.19: Intermodulation products of two-tone test.

The difference and the sum of the original input singals create second and third order IMD products and harmonics. When the two original input signals are at the frequency of f_1 and f_2, second order IMD products will appear at f_2 - f_1 and f_1 + f_2. In the same manner third order IMD products will rise at $2f_1$ - f_2 and $2f_2$ - f_1. Second and third order harmonics are not depicted in the figure 2.19, however, they are basically the products of the original signals at $2f_1$ and $2f_2$.

IMD products are the result of distortion which lower the system performance. Therefore, it is confirmed that there is a trade-off between linearity and efficiency. High linearity requires sacrifice from efficiency. Hence, it is an important parameter that needs to be taken care of when designing a PA.

2.3.6 Noise Figure

The Noise Figure (F) is a parameter of noise performance in an LNA in the receiver and it is defined as input and output differences in the signal power level and noise power level. It is expressed by the following formula:

$$F = \frac{P_{Si}/P_{Ni}}{P_{So}/P_{No}} \tag{2.28}$$

where P_{Si} is input signal power level, P_{Ni} is input noise power level, P_{So} is output signal power level, and P_{No} is output noise power level. Noise figure of an LNA represents the available gain of the same system. In other words, a high noise figure means that the LNA is providing low gain.

2.3.7 Peak-to-Average Power Ratio (PAPR)

The ratio of the peak signal power to average signal power is another important parameter when designing PAs. PAPR is expressed by the following formula.

$$PAPR = 10\log\left(\frac{P_{peak}}{P_{average}}\right) \tag{2.29}$$

High PAPR signals play a major role in modern communication systems since they can provide high data rate transmission. Conventional PAs when used in high PAPR systems suffer from low average power which causes low efficiency in overall system [4, 8, 42]. Hence, efficiency enhancement techniques for PA design are becoming more important to investigate in both academia and industry.

2.4 Efficiency Enhancement Techniques for PA

In the traditional PA design, maximum efficiency is provided at the maximum output power level. However, operating at this level creates distortion. In order to overcome distortion, PA can operate at the back-off power level but this leads to efficiency decrease. Hence, several methods have been introduced to enhance the efficiency of PA. In this section, only four of them will be explained. These methods are Envelope Elimination and Restoration (EER), Envelope tracking (ET), Outphasing, and Doherty Technique [3,5,43]. The Doherty technique is selected to study and implement as an efficiency enhancement technique to improve the amplifiers in this study. Therefore, it will be discussed in section 2.5 seperately.

2.4.1 Envelope Elemination and Restoration

The EER was introduced by L. Kahn in 1952 as an efficiency enhancement method. The methodology here involves exploiting non-linear and high efficiency PA with low-frequency-limiting amplifier which results in the elimination of the envelope [21, 44].

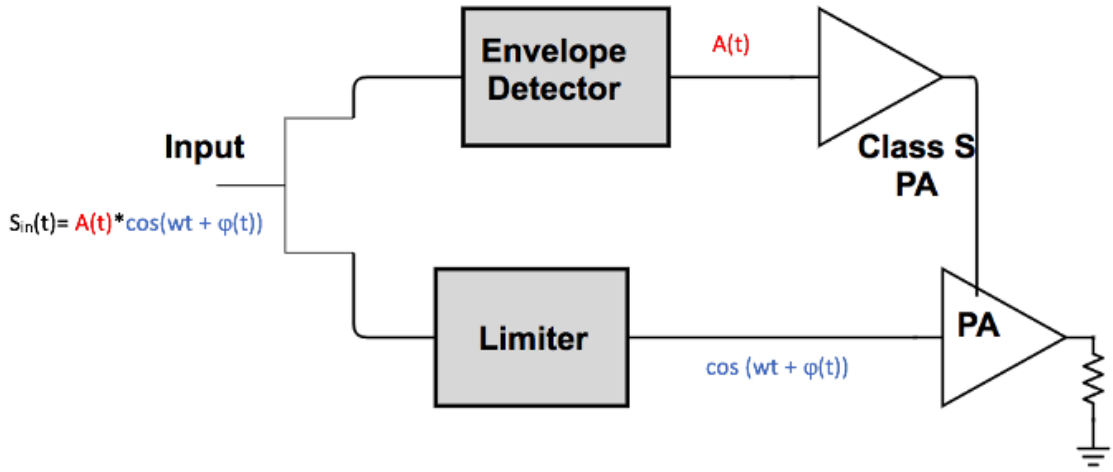


Fig. 2.20: EER block diagram.

Figure 2.20 [45] represents the block diagram of the EER method. Here the input signal is splitted into phase and amplitude by a limiter and an envelope detector. At the limiter

output, phase component of the signal (ϕ(t)), which has a constant amplitude and modulated phase, is amplified by high efficiency and non-linear amplifier (biased at C, E, or F). At the envelope detector output, the constant amplitude component of the signal (A(t)) is amplified by non-linear S-class amplifier to increase its efficiency. Then, A(t) is combined at the output with ϕ(t) by modulating the supply voltage (V_{dd}) of the amplifier [46]. Even though this method provides increased efficiency, in theory, practical implementation of this method has its disadvantages. For instance, splitted RF input signal components follow two different paths by passing two different circuitries. Therefore, there could be possible mismatch when combining both. Moreover, dynamic range is required for the supply modulator as well as large bandwidth.

2.4.2 Envelope Tracking

ET is another method used to enhance the efficiency of the PA when the input signal is not splitted as in EER. Figure 2.21 [45] shows the ET block diagram. In this method, unlike EER, a limiter and a high efficient, a non-linear PA is not employed. Instead, ET exploits a DC-DC converter as a modulator to adjust the voltage transferred to PA. Thus, PA runs at the maximum efficiency. [22].

One of the important points in the application of the ET method is that the PA should be linear since a non-constant signal is amplified. Thus, PA used in this case should operate in class A, class B, or class AB. Performance comparison between ET and EER shows that ET has better linearity than EER. However, EER provides higher efficiency.

There are a couple of drawbacks to this method. First, accurate timing is required between envelope modulation and dynamic ET supply. Second, to modulate the necessary voltage, large bandwidth DC power supply is required.

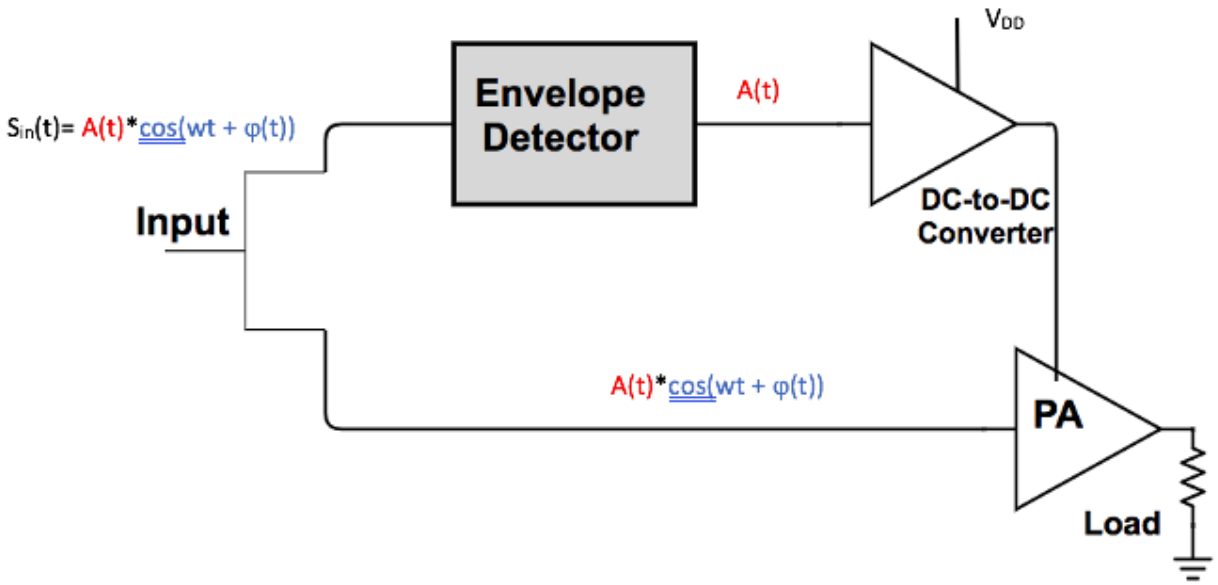


Fig. 2.21: Envelope tracking block diagram.

2.4.3 Outphasing

The outphasing was introduced by H. Chireix in 1935 [23]. This method is also known as Chireix outphasing. Figure 2.22 [45] shows the block diagram of outphasing. In this method, two RF input signals with different phases are amplified by two non-linear amplifiers. Then, the two signals are combined at the output to reform the signal [47,48]. Theory

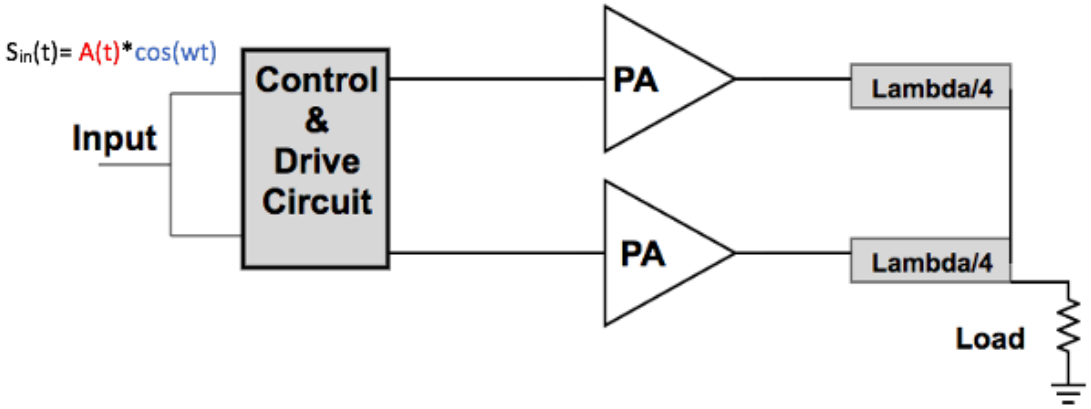


Fig. 2.22: Outphasing (Chireix) block diagram.

of this method is explained in detail with mathematical expressions in [5].

Briefly, an amplitude modulated RF input signal S_{in}(t) is applied to a phase modulator using trigonometric identity,

$$\cos(A) + \cos(B) = 2\cos\left(\frac{A+B}{2}\right).\cos\left(\frac{A+B}{2}\right) \tag{2.30}$$

if the amplitude modulated input signal is given by,

$$S_{in}(t) = A(t).\cos(wt) \tag{2.31}$$

Then, the generated amplitude signals S_1(t) and S_2(t) will be derived as following,

$$S_1(t) = \cos\big(wt + \cos^{-1}(A(t))\big) \tag{2.32}$$

and

$$S_2(t) = \cos\big(wt - \cos^{-1}(A(t))\big) \tag{2.33}$$

Therefore, the mathematical expression for the combined output signal is given as,

$$S_{out}(t) = G.(S_1(t) + S_2(t)) = 2.G.A(t).\cos(wt) \tag{2.34}$$

where G is the voltage gain of the amplifier. Two signals at the output have different phases. Thus, conventional power combining methods might lead to losses. To overcome this issue, a reactance compensation load which helps to have better efficiency in the back-off power level is applied. The disadvantage of this method is the selection of shunt reactance and the lack of proper design requirements.

2.5 Doherty Technique

Classical PA designs suffer from low overall efficiency. PAs can deliver peak efficiency when the output power is at maximum. To overcome this issue, several efficiency enhancement techniques have been studied such as EER, ET, Outphasing, and the Doherty technique.

In 1936, W. H. Doherty introduced a new method for signal amplification [24]. In this technique, two vacuum tubes and an impedance matching network were used to achieve a new type of linear amplifier for radio-frequency (RF) applications. This new method did not draw much attention until late 80s when F. H. Raab outlined theoretical approach of instantaneous efficiency for DPA over a wide range of output power level [43]. Since then DPA has become very popular for wireless communication systems due to its simplicity and ability to provide high efficiency with extended power range. [49–51].

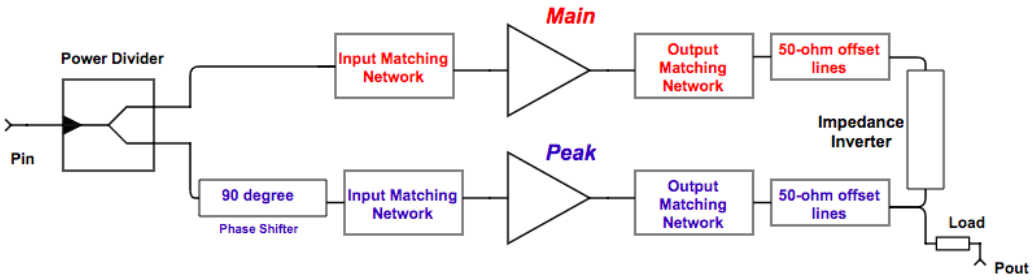


Fig. 2.23: Doherty power amplifier block diagram.

The modern DPAs consist of two amplifiers; the main amplifier biased in Class AB and the peak amplifier biased in Class C. Figure 2.23 shows the conventional DPA block diagram. Besides active devices, main and peak amplifiers, there are other components in the system such as, power divider, quarter wave transmission lines, input matching network, output matching network and power combiner.

A quarter wavelength transmission line connects the main amplifier to the peak amplifier. The power divider splits the signal into two and the combiner converts the boosted signal and transfers it to the output load. DPA operation principles have been studied in

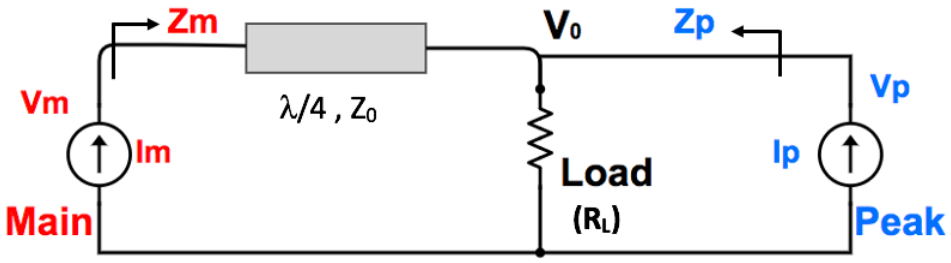


Fig. 2.24: Doherty power amplifier circuit schematic.

detail in the literature [4, 5, 52]. Therefore, in this work, the basic theory will be described briefly. Figure 2.24 shows circuit equivalent of conventional DPA. The following expressions are describing how the load is modulated in these method. Here, the current and voltage of the main amplifier are I_m and V_m where as I_p and V_p are the current and voltage of the peak amplifier. Also, the load is represented by R_L. There is a quarterwave length ($\lambda/4$) impedance inverter with the charactereristic impedance (Z_0) of 50-ohm which compensate the phase shift between main and peak amplifier. Mathematically, this impedance inverter can be represented as matrix [40].

$$\begin{bmatrix} V_m \\ I_m \end{bmatrix} = \begin{bmatrix} 0 & jZ_0 \\ \frac{j}{Z_0} & 0 \end{bmatrix} \begin{bmatrix} V_0 \\ \frac{V_p}{R_L} + jI_p \end{bmatrix} \tag{2.35}$$

Where V_p is equal to V_0 and I_p is replaced with the complex value of -jI_p. Consequently, voltages of the main and peak amplifiers can be obtained from equation 2.35 as following:

$$\begin{bmatrix} V_m \\ V_p \end{bmatrix} = \begin{bmatrix} \frac{Z_0^2}{R_L} & -jZ_0 \\ -jZ_0 & 0 \end{bmatrix} \begin{bmatrix} I_m \\ -jI_p \end{bmatrix} \tag{2.36}$$

The impedances seen from the main and peak amplifiers can be formulated as the following expressions.

$$Z_m = \frac{V_m}{I_m} = \frac{Z_0^2}{R_L} - Z_0 \frac{I_p}{I_m} \tag{2.37}$$

$$Z_p = \frac{V_p}{I_p} = Z_0 \frac{I_m}{I_p} \tag{2.38}$$

Therefore, main and peak amplifiers voltages can be derived from equations 2.37 and 2.38.

$$V_m = Z_0(I_m \frac{Z_0}{R_L} - I_p) \tag{2.39}$$

$$V_p = V_o = -jZ_0 I_m \tag{2.40}$$

Impedances seen by the main and peak amplifier show that current sources of both main and peak amplifiers have a load modulation because of their presence. The voltage gate source ,V_{gs}, is the parameter that controls the current of main and peak amplifiers. Thus, the current values of both amplifiers can be expressed by the following:

$$I_m = \begin{cases} 0 & \text{if } V_{gs} < 0, \\ G_m V_{gs} & \text{if } 0 \leq V_{gs} \leq V_{gs,max}, \\ G_m V_{gs,max} & \text{if } V_{gs} > V_{gs,max}. \end{cases} \tag{2.41}$$

$$I_p = \begin{cases} 0 & \text{if } V_{gs} < \alpha V_{gs,max}, \\ G_p(V_{gs} - \alpha V_{gs,max}) & \text{if } \alpha V_{gs,max} \leq V_{gs} \leq V_{gs,max}, \\ G_p(1-\alpha) V_{gs,max} & \text{if } V_{gs} > V_{gs,max}. \end{cases} \tag{2.42}$$

$V_{gs,max}$ is the maximum gate voltage that the device can handle and α is a back-off parameter. Also, the transconductance of the main and peak amplifiers are represented by G_m and G_p, respectively.

In the low power region, the main amplifier is active since V_{gs} <$\alpha V_{gs,max}$ and the peak amplifier is off (I_p = 0). Thus, impedance and voltage parameters of the main amplifier can be shown as:

$$Z_m = \frac{Z_0^2}{R_L} \tag{2.43}$$

$$V_m = I_m \frac{Z_0^2}{R_L} \tag{2.44}$$

In the low power region, V_{gs} = $\alpha V_{gs,max}$ which is the back-off point, the main amplifier gets saturated. Therefore, V_m becomes:

$$V_m = G_m V_{in} \frac{Z_0^2}{R_L} = G_m \cdot \alpha V_{in,max} \cdot \frac{Z_0^2}{R_L} = V_{dc} \tag{2.45}$$

In the high power region, the peak amplifier becomes active since V_{gs} >$\alpha V_{gs,max}$ and both amplifiers contribute at the output power. Therefore, the voltages for main and peak amplifiers can be shown as:

$$V_m = I_m Z_m = I_m \left(\frac{Z_0^2}{R_L} - Z_0 \frac{I_p}{I_m} \right) = V_{dc} \tag{2.46}$$

$$V_p = I_p Z_p = I_p \left(Z_0 \frac{I_m}{I_p} \right) = I_m Z_0 \tag{2.47}$$

These analyses are the fundamentals of DPA design and help designers to understand the behavior of both amplifiers in each region. Therefore, these formulations are the starting point and will be utilized in practical applications.

The efficiency of conventional DPA is depicted in [53]. As Figure 2.25 illustrates, DPA has three regions of operation. In the low power region, the peak amplifier stays inactive due to its Class C bias and acts as an open circuit. This causes the main amplifier's load impedance to be doubled by quarter wavelength ($\lambda/4$) impedance inverter. Fig. 2.26 depicts an equivalent circuit diagram for low power region.

As the main amplifier reaches its saturation point, the system goes into medium power region where the peak amplifier turns on as shown in circuit diagram in Fig. 2.27. Load impedance starts decreasing for the main amplifier as the peak amplifier introduces current to the load. As current increases for the peak amplifier, load impedance of the combiner

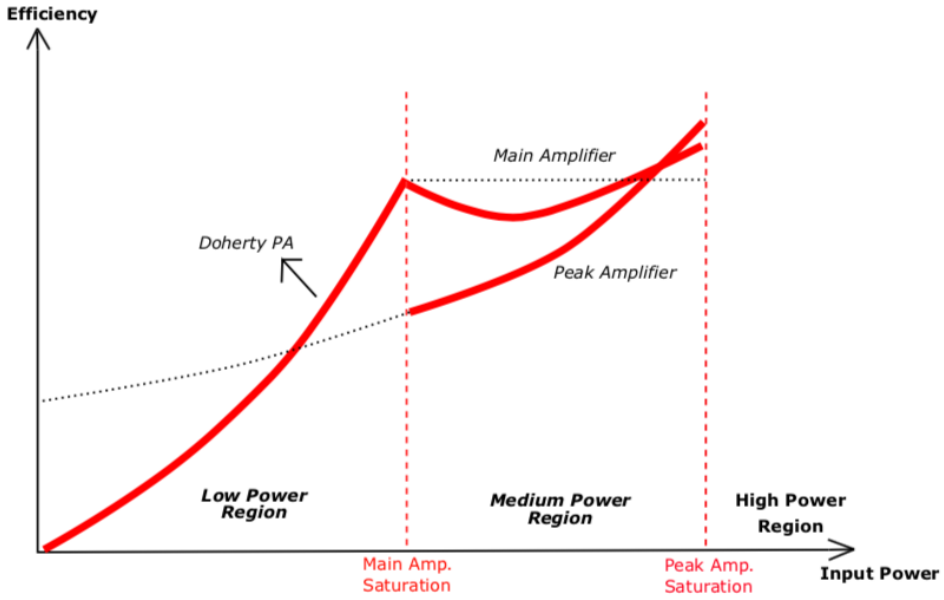


Fig. 2.25: Efficiency vs input power.

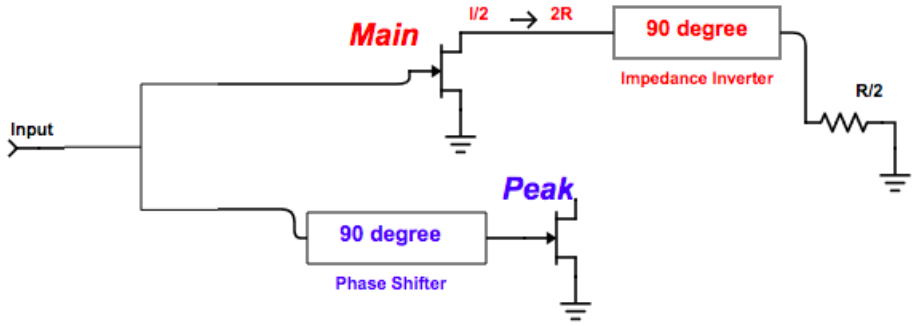


Fig. 2.26: Equivalent circuit diagram for low power region.

network increases and it causes total output power to increase.

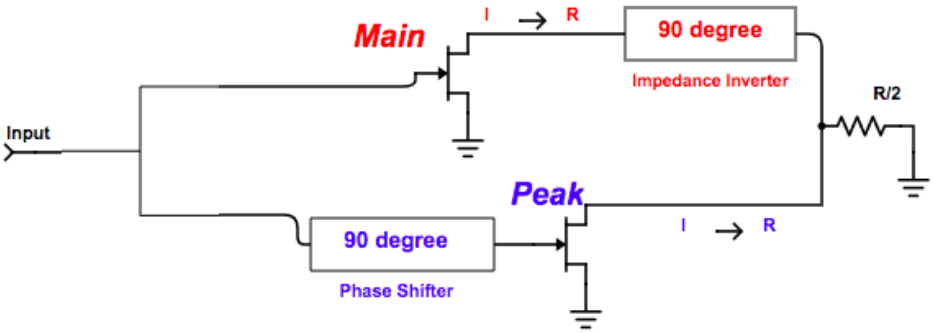


Fig. 2.27: Equivalent circuit diagram for medium power region.

In the high power region, both amplifiers operate close to their saturation point. DPA improves the linearity at the high power region by the saturation of the main amplifier and the peak amplifier.

DPAs are suitable for wireless communication systems' designs for different applications and technologies, however, they are mostly used in base stations and frequency range of 0.5 - 4 GHz which are L- and S- band.

Previously, there have been reviews on DPA designs. In [54], the theoretical perspective of DPA was discussed, where the conventional DPA structure with Class AB biased for the main amplifier and Class C for the biased the peak amplifier was used to analyze the DPA topology. Historical aspects of the Doherty technique in PA designs and modern topologies of DPA including N-stage and N-way structures were reviewed in [50]. In the subsequent years, [51] was published as a contuniation to [50], where DPA applications and technologies were outlined. Additionally, linearity and efficiency techniques are explained. Most importantly, bandwidth limitations and multiband solutions were discussed. These review papers cover developments on DPA to some extent up until 2015. In two of the more recent survey studies, the reflection of mobile handset applications and 5G standards for DPA [55] and dual-band DPA for next generation communication systems were reviewed [56].

Although there are several advantages of the Doherty technique as an efficiency enhancement method, it suffers from nonideal transistor behavior and some other design limitations. These are namely imbalanced gain, imbalanced phase, output power leakage, and bandwidth [57]. Conventional DPA has non-identical bias points for the main and the peak amplifiers, which lead to different output power levels and ultimately imbalanced gain for amplifiers. Possible solutions might be proposed for this issue such as uneven power drive, multi-way or multi-stage design, different transistor for the main and the peak amplifiers and optimized input and output matching circuits [58]. The imbalanced phase is another practical challenge caused by different classes of operations between the main and the peak

amplifiers. This power-related phase imbalance situation specifically occurs in the output combiner of the DPA design when GaN used [59].

As explained, the peak amplifier is not active in the low-power region and should act like an open circuit. Therefore, there should not be any power flow to the peak amplifier from the main amplifier. However, due to parasitic elements of the transistor, output power flows into peak amplifier and causes power loss, which ultimately decreases the efficiency.

In [60], the proposed method uses 3-dB hybrid coupler as an output combiner network for both the main and the peak amplifiers instead of designing individual output matching networks. Proof of concept is designed using Cree CGH60008D with 28 volt bias voltage operating from 1.95 GHz to 2.25 GHz. Measured results show that proposed design provides 42 dBm output power with 65% efficiency and with 15 % fractional bandwidth.

In [61], the authors outline theoretical and practical limitations. The theoretical limitation is mainly caused by the quarter wave length transmission lines of the output impedance inverter. Transistors used in the main and the peak amplifiers also have an effect on this as they have different current profiles. Proposed theory requires to terminate the main amplifier to produce a good modulation. In the conventional DPA, the ratio of the currents for the amplifiers(Im/Ic) is equal to 1. Therefore, in order to have proper modulation the main amplifier should have half the load than the peak amplifier. In this case, even though efficiency decreases at 6 dB OBO, bandwidth increases.

The practical limitation is mostly about the length of offset lines, which is actually a dilemma because the performance of DPAs also depend on offset lines. To solve this problem, authors' suggestion is to design a combined impedance transformer instead of having seperate output matching networks. However, this would be challenging due to the different bias points of the main and peak amplifiers.

2.6 Transistor Technologies for PA

Wireless communication systems require PAs with high efficiency, good linearity, and improved bandwidth for microwave applications. Therefore, designing optimum performance amplifiers has become an important task to perform. The selection of an active device is the first step of the design process. Transistor choice depends on the system requirements and material characteristics of the device. There are several commercially available technologies, such as Silicon-Laterally Diffused Metal Oxide Semiconductor Field Effect Transistor (Si-LDMOS), Silicon (Si), Silicon Carbide (SiC), Gallium Arsenide (GaAs), and Gallium Nitride (GaN).

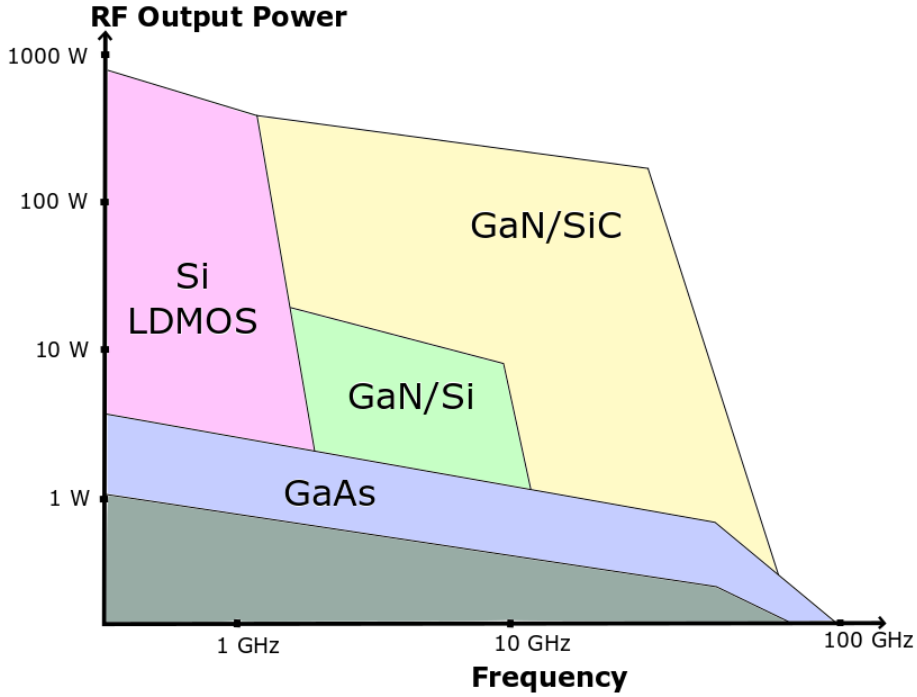


Fig. 2.28: Transistor technology comparison: RF output power vs. frequency.

Si-LDMOS transistors have been dominant because of their low-cost and availability for high-power and low-frequency applications such as base-station. Si-LDMOS transistors might be a good alternative to systems operating at L-band and provide RF output power up to 120 W with 28-volt power supply. GaAs devices are used in low-power, high-frequency,

and low-noise microwave applications such as satellite communications. GaAs transistors have a larger package size and low operating voltages in comparison to GaN. Therefore, they are not a good fit for high power applications. GaN transistors deliver high-power and high voltage at high frequencies with higher power added efficiency compared to Si-LDMOS and GaAs transistors [3, 62–64]. Figure 2.28 [63] shows output power level of different transistors over frequency range.

Transistor Properties	Transistor Technology			
	Silicon (Si)	SiC	GaAs	GaN
Dieletric Constant	11.9	9.8	12.5	9.5
Bandgap (eV)	1.12	2.86	1.42	3.4
Electron Mobility (cm^2/v-sec)	1300	650	5000	1500
Thermal Conductivity(W/cm-K)	1.3	4.9	0.46	1.3
Breakdown field(V/cm)	0.3	2	0.4	2

Table 2.2: Transistor Material Properties

These are important parameters to pay attention while selecting a transistor such as bandgap, electron mobility, breakdown field, and thermal conductivity. Table 2.2 compares the characteristic material properties of different technologies. A wide bandgap leads to a higher power density which leads to a higher efficiency. GaN has a value of 3.4 eV whereas GaAs has a value of 1.42 eV. High electron mobility helps to have high frequencies. GaAs electron mobility is 5000 cm2/V-sec which is more than three times higher than GaN. High breakdown field allows to have high voltage which improves the efficiency and gain.

Additionally, high thermal conductivity helps to achieve higher temperature [65, 66]. Therefore,in short, properties that are showing the advantages of GaN transistor are mainly, high break down voltage, wide band gap, high thermal conductivity, and high current density.

Another indicator of GaN transistors for becoming a better fit for the communication systems is the market share and forecast for transistor technology. According to Yole Technology and Market report [67], the GaN market share for defense and communication industry was $12 million in 2016. The market share is estimated to have an exponential

growth and reach $2 billion by 2024 [68]. One of the main reasons why and how GaN is the rising star among available transistor technologies is its high power and high efficiency operating capability at high frequency. Although GaN still has high cost compared to Si-LDMOS and GaAS, it is projected that GaN will replace Si-LDMOS in the cable tv market and GaAs in the satellite communication industry.

In light of this, GaN technology is a better alternative than other technologies for high efficiency, high power, and high temperature at high-frequency operations because of its smaller size and steady performance.

CHAPTER 3
A LOW-NOISE AMPLIFIER (LNA) DESIGN AT 2 GHZ

3.1 Introduction

Especially with the improvement in cellular communication and wireless connection, RF front-end devices have been receiving increased attention to design an amplifier that operates over wideband as the frequency spectrum is overwhelmingly used. Hence, the design of a wideband low-noise amplifier (LNA) has been an important research field for years.

In [69], the design aims to achieve a minimum noise figure by having a mismatch in the input matching circuit. However, the design has lower gain because of the mismatch. Besides, the defined value of source inductance helps to keep noise figure level low as it gives series of feedback to the system. The reported measured noise figure is less than 1 whereas the overall gain is around 14.8 dB with the input return loss of 9.8 dB.

[70] presents a method where the current feedback and unilateralization are used to have low noise at the low current levels. The design is able to provide 15 dB gain and 1.3 noise figure.

In [71], the BJT LNA design operating at 1 GHz is presented. The cascode configura-

tion is applied and inductive emitter degeneration is used. Even though the design yields a low noise figure of 0.359, its power gain is at 3.3 dB with the input return loss of 6 dB.

In [72], there are two designs. the first one is following the conventional LNA design procedure and the second one is focused on the effects of grounding vias and transistor pads. The second design provides a noise figure of 1.5 with a gain of 16 dB and a return loss around 15 dB.

Another design using the cascode approach is [73]. In this design, the shunt-series input matching circuit is also proposed and the design was able to achieve a noise figure of 1.87 with an overall gain of 14.3 dB.

In [74], the proposed design is operating at 2.3 GHz and providing 1.1 dB noise figure, 15.11 dB gain and 19.2 dB input return loss at the center frequency. The methodology applied in this design is based on inductive source degeneration to design inductively loaded amplifier.

A linearization technique is analyzed in [75] . The approach here is to terminate the input of the amplifier with a lower impedance at the low frequencies of the second order harmonics. This approach is validated on BJT, however, for FET, it is not effective as in BJT. Proposed design provides a noise figure of 1.4 dB and gain of 15.7 dB

Another LNA design with BJT is presented in [76]. The proposed amplifier utilizes the current-feedback method and shows that out of band termination for an LNA helps to increase linearity. This approach is validated with experimental results. The LNA provides 15 dB gain and 1.3 dB noise figure at the center frequency of 0.9 GHz.

In [77], reported LNA is utilizing the dual feedback approach by adding capacitors at the input and output. The LNA oparates at the center frequency of 2.1 GHz and provides 1.65 dB noise figure. In [78], the theorectical approach is presented in order to decrease in phase noise. The impact of active feedback at low frequencies studied and mathematical expressions are derived.

3.2 Proposed Design

In this work, a wideband low-noise transistor amplifier is designed based on microstrip technology. The design methodology is to define the optimum input and output reflection coefficients to achieve maximum unilateral transducer gain. The optimum reflection coefficients (Γ_S and Γ_L) are calculated for both the input matching network (IMN) and the output matching network (OMN) appliying the equations provided in section 2.1. Both networks are realized using distributed elements (symmetrical open circuit stubs). Lumped elements (R-L-C) are not preffered in the network designs due to their complexity and parasitic effects of these elements. Furthermore, a passive DC bias network is utilized to ensure good transmission from source to the load. This design is simulated, fabricated, and tested. The circuit simulations are performed using Microwave office AWR Design Environment [79] and electromagnetic (EM) simulation is carried out by Sonnet Software [80].

The circuit was built on a 0.5-ounce, 60-mil substrate, Roger 4003C [81], with dielectric constant ϵ_r of 3.55 and loss tangent γ of 0.0027. Measured results include the S-parameters, the noise figure, and the two-tone response of the amplifier. They are in good agreement with the simulation results. The measured gain is within 1 dB of 13.84 dB over the frequency range from 1.75 GHz to 2.25 GHz. The noise figure is about 1.6 dB over 1.9-2.2 GHz band. The input return loss is greater than -10 dB over 1.7-2.1 GHz. The output return loss is better than -5 dB over 1.7-2.3 GHz.

Figure 3.1 shows the block diagram of the proposed LNA. The first step of the design of an LNA is defining the transistor's stable region by plotting input and output stability circles and choosing the reflection coefficients Γ_S and Γ_L such that the specified stability, gain, noise figure, bandwidth, and input/output VSWRs are achieved. The second step is designing the input and output matching networks that produce the chosen Γ_S and Γ_L.

The selected transistor for this project is NXP-BFG425W [82] with the biasing conditions of $V_{CE} = 2V$ and $I_C = 25mA$. It provides high power gain, low noise figure, and low feedback capacitance. It is a surface-mount package (SOT-343R) with four pins and

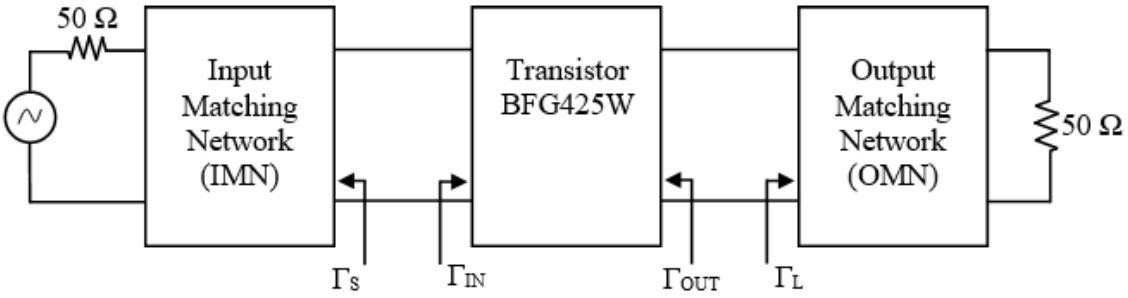


Fig. 3.1: The LNA block diagram at 2 GHz.

suitable choice for RF front-end and wideband applications.

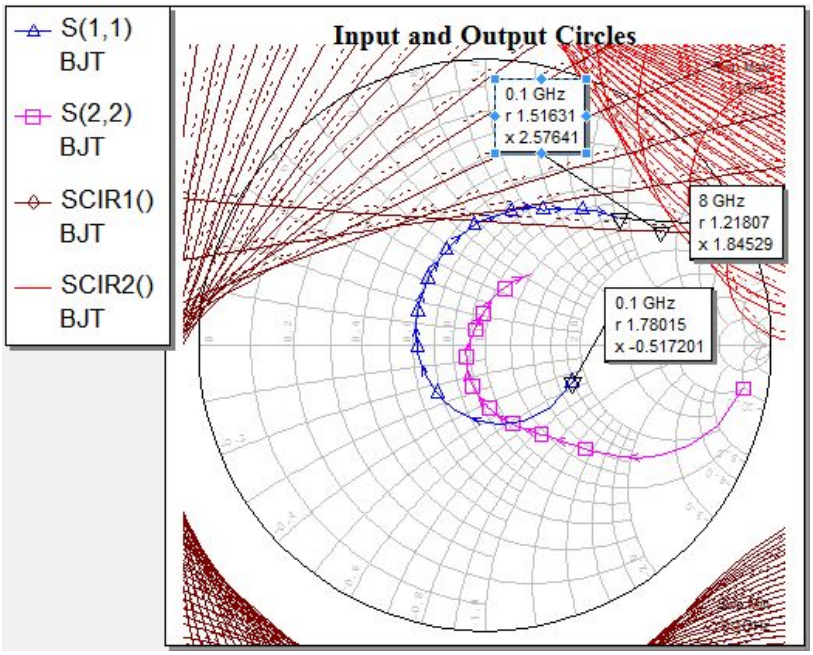
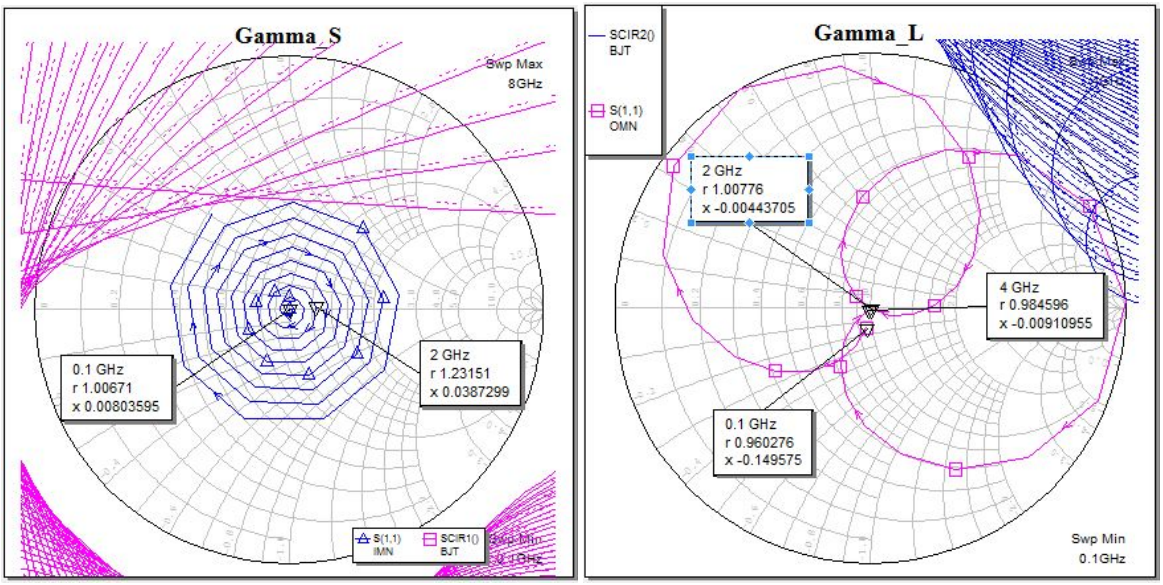


Fig. 3.2: Input and output stability circles of the chosen transistor.

This transistor is unconditionally stable above 0.1 GHz as shown in Figure 3.2. After plotting the input and output stability circles of the chosen transistor, Γ_S and Γ_L are selected such that they are not in the transistor's unstable region over all frequencies as depicted in Figure 3.3.

Figure 3.4 shows the complete schematic of the propsed LNA. The schematic is created in a computer aided design tool, Microwave Office AWR Design Environment. Both input and output matching networks are realized using open-ended stubs. The initial length and



(a) Γ_S (b) Γ_L

Fig. 3.3: Γ_S and Γ_L points on the Smith chart.

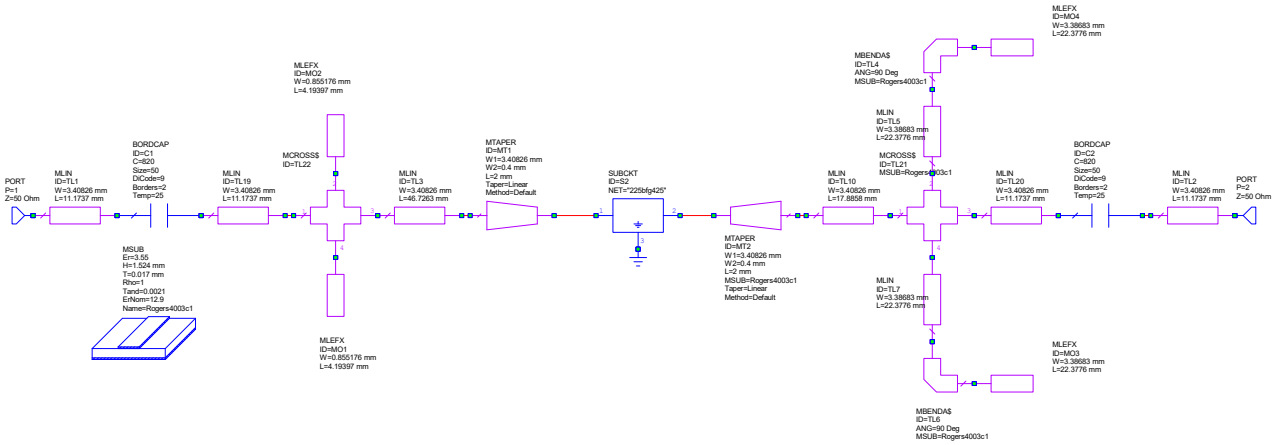
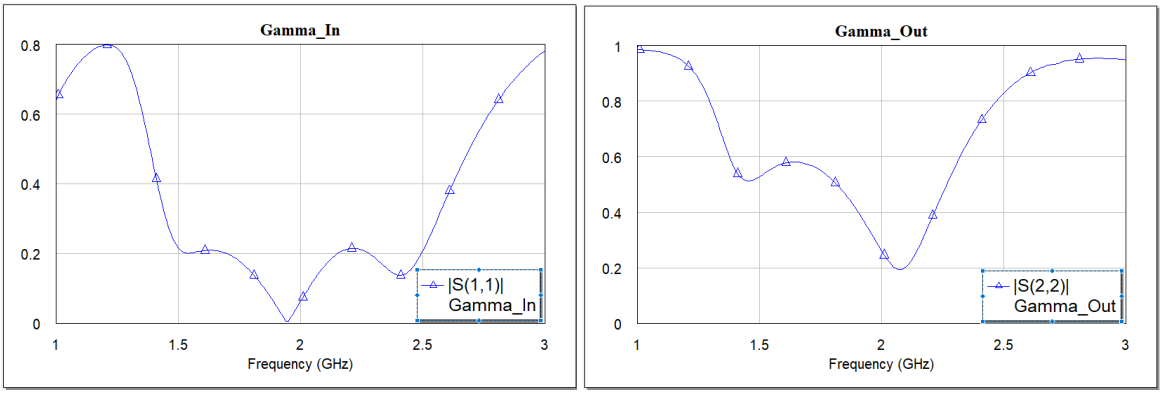


Fig. 3.4: Complete circuit schematic of the proposed LNA.

width of the open-stubs and transmission lines were adjusted in circuit simulation tools.

After circuit simulation and optimization are completed, input and output return losses results showed that the design is performing as expected. Figure 3.5 presents the absolute value of input return loss (S_{11}) and output return loss (S_{22}) of the overall ampilifer, respectively. Both results show that over the desired frequency band, (S_{11}) and (S_{22}) are less than 0.4 which is much smaller compared to the oscillation value of 1. This shows that a stable design is achieved.



(a) (b)

Fig. 3.5: Γ_{IN} and Γ_{OUT} of overall amplifier.

Figure 3.6 shows the input and output voltage standing wave ratio from the circuit simulation. Both values are less than 2 over the desired frequency band.

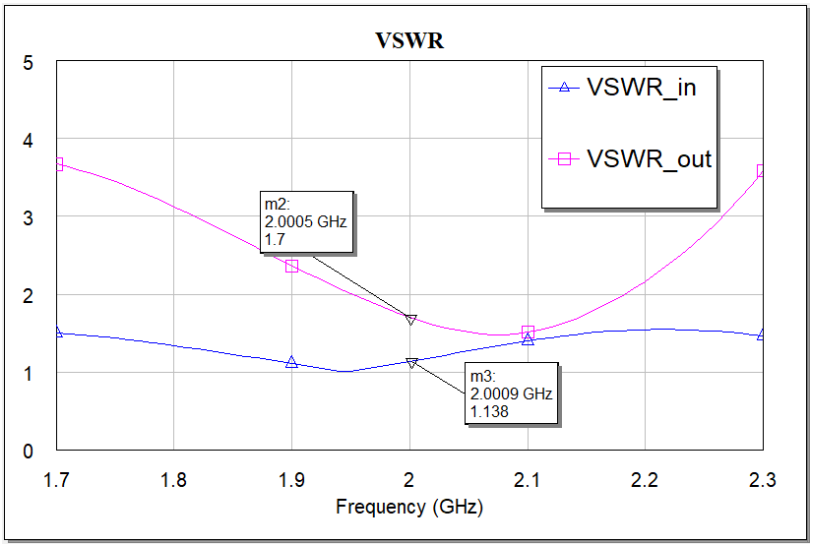


Fig. 3.6: Circuit simulation of input and output VSWR.

Figure 3.7 provides circuit simulation results of the overall gain of the LNA which is over 17 dB between 1.7-2.3 GHz. NXP-BFG425W [82] data sheet notes that this transistor might achieve the maximum gain of 18 dB. Thus, the circuit simulation results show that the design performs well under the ideal environment.

After completing initial design in the circuit simulation tool AWR, the design layout was exported from circuit simulation program as a DXF file and imported into the Sonnet

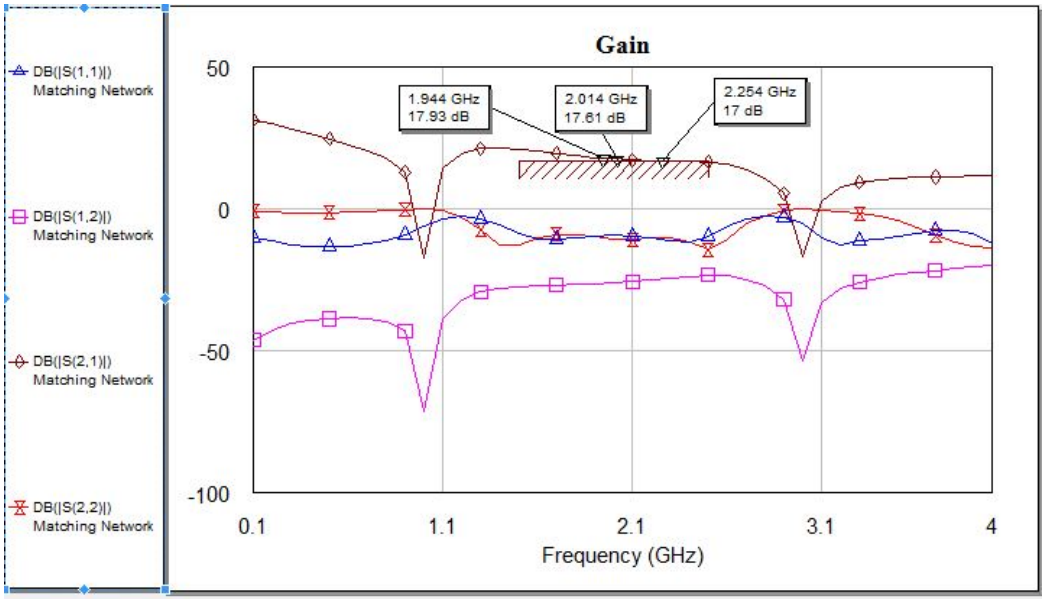


Fig. 3.7: Circuit simulation of overall gain of the LNA.

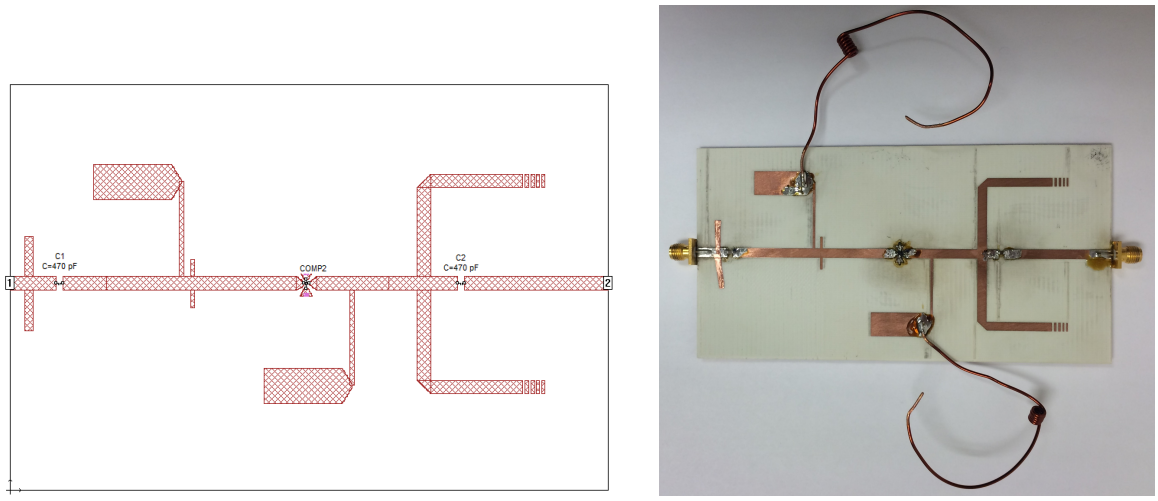
Software. The length and width of the components of the circuit were finalized and optimized in the Sonnet Software for the EM simulation. For DC blocking purposes, 470 pF capacitors were used at both IMN and OMN. The open-stub in OMN was relatively long as shown in Figure 3.4. Each DC bias network consists of a low impedance quarter wavelength line connected to a high impedance quarter wavelength line that is attached to the main line. Figure 3.8 (a) illustrates the mentioned bias networks.

3.3 Experimental Results

The circuit was fabricated using the LPKF ProtoMat S103 [83] milling machine at the Microwave Lab at Syracuse University. The image of the complete fabricated circuit is shown in Figure 3.8 (b).

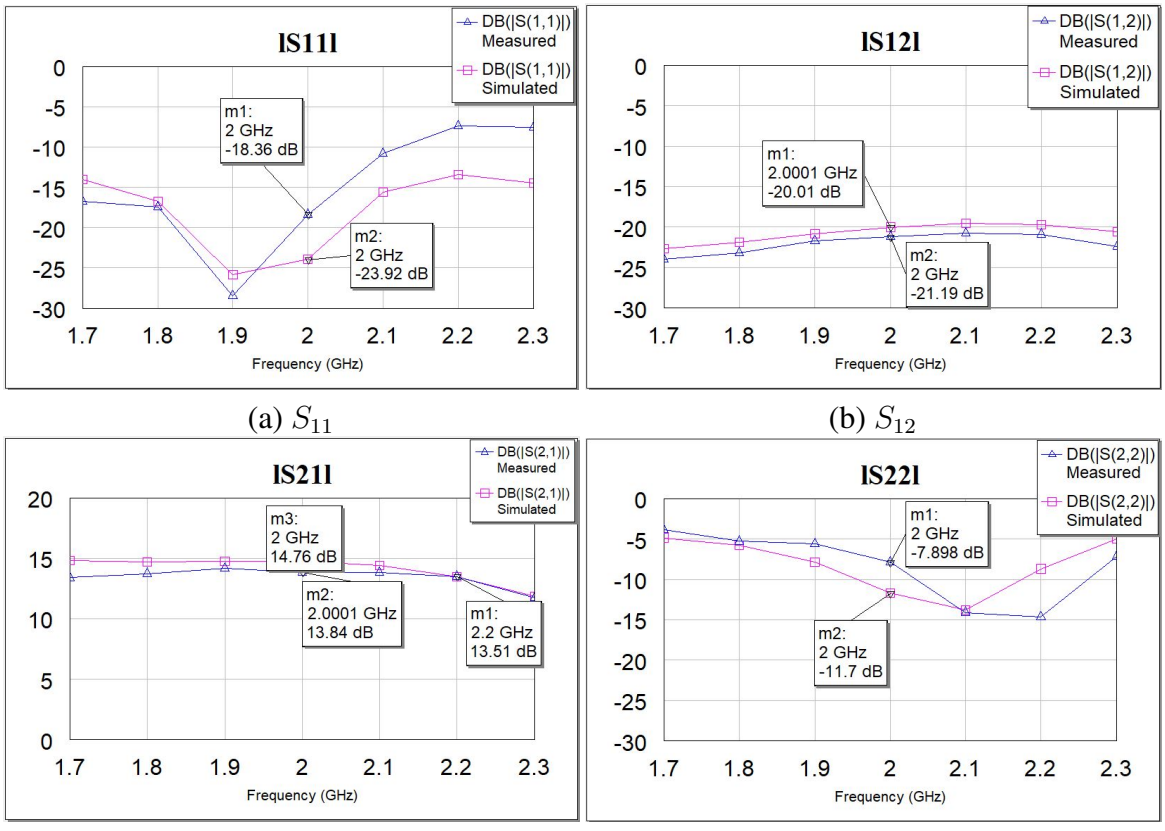
The EM simulations were run in Sonnet Software and presented in figures below with the measured results. Network analyzer, spectrum analyzer, signal generator, and noise figure analyzer were used to measure the results after fabricating the circuit.

As shown in Figure 3.9, simulated and measured S-parameter results have a similar



(a) Circuit layout (b) Fabricated circuit

Fig. 3.8: Low-Noise amplifier at 2 GHz.



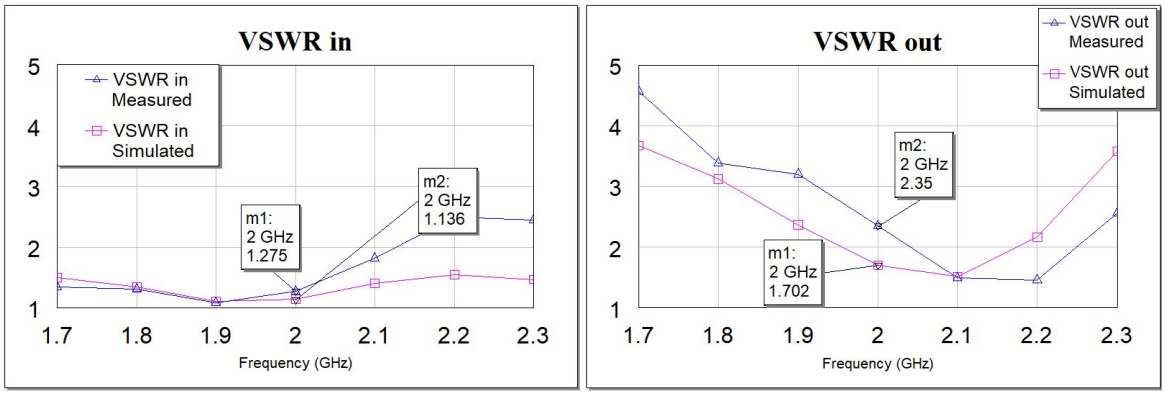
(a) S_{11} (b) S_{12}

(c) S_{21} (d) S_{22}

Fig. 3.9: EM simulated and measured S-parameters

pattern. Measured input return loss (S_{11}) is -18.36 dB whereas simulated S_{11} is 23.92 dB. On the other hand, measured Output Return Loss (S_{22}) is -7.89 dB while simulated S_{22} is

11.7 dB at the center frequency. For the gain (S_{21}) of the LNA, it can be observed that the amplifier has measured gain of 13.84 dB gain with ± 1 dB over 1.75 GHz to 2.25 GHz frequency range whereas the simulated gain is 14.78 dB. Simulated and measured input values of VSWR are 1.136 and 1.275 respectively.



(a) Input VSWR (b) Output VSWR

Fig. 3.10: EM simulated and measured VSWR

Even though there is a slight difference between simulation and measured results, they show similar patterns. On the other hand, output VSWR has slight difference as depicted in Figure 3.10. Simulated value is 1.702 while measured value is at 2.35. The differences between the EM simulation and measurement results are related to fabrication steps and might be overcome with the second build with carefull process.

Figure 3.11 illustrates that the LNA has minimum noise figure of 1.615 dB at 2 GHz. From 1.75 GHz to 2.2 GHz we have relatively similar values. The data sheet of NXP-BFG425W [82] provides the typical value of noise figure at 2 GHz with the biasing condition of $V_{CE} = 2V$ and $I_C = 25mA$ as greater than 2. Having a better noise figure is a result of sacrificing from other parameters such as gain and output VSWR.

Another parameter that should be taken into account when designing an amplifier is 1-dB gain compression point, P1dB. Basically, it determines the point where the amplifier becomes non-linear. Figure 3.12 shows that 1-dB gain compression point might be achieved when the input power sweep has the value of 0.5 dBm. In order to show the de-

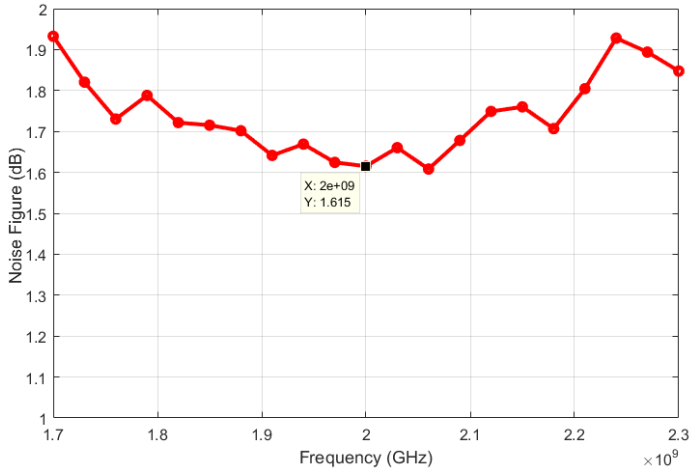


Fig. 3.11: Noise figure of the LNA

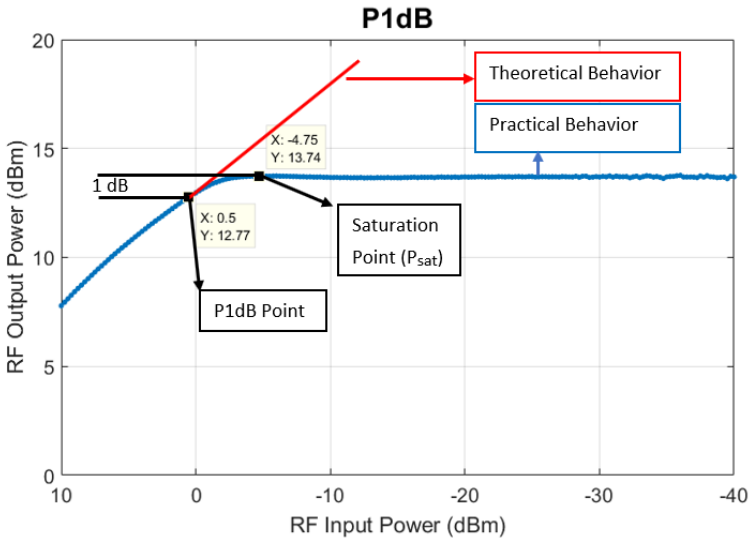


Fig. 3.12: 1 dB compression point

gree of non-linearity of the amplifier, two-tone intermodulation distortion test is applied. Two signal generators that produce the same power level were applied to the input. The output was observed on the spectrum analyzer as shown in Figure 3.13. When both input signals were above -30 dBm, only two peaks around our center frequency were observed. As the input level increased to -18 dBm, third order inter-modes appeared as presented in Figure 3.14.

Table 3.1 shows the performance comparison of the reported studies that use various

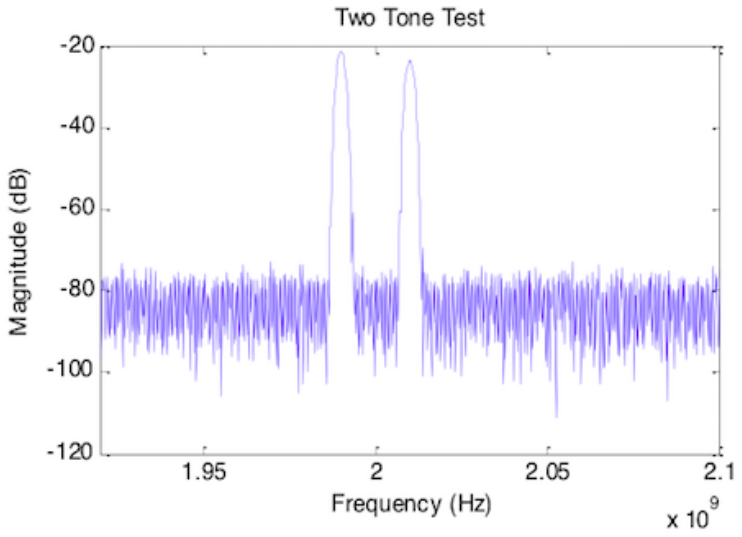


Fig. 3.13: Two-tone test

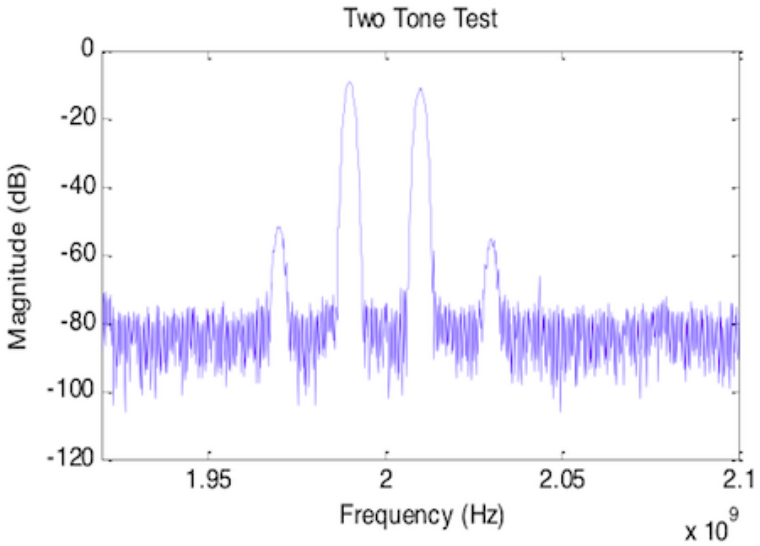


Fig. 3.14: Third-order intermodes

Reported Studies	Transistor Model	Frequency (GHz)	Noise Figure (dB)	Return Loss (dB)	Gain (dB)	Bandwidth (MHz)
This work	**NXP-BFG425N**	**2**	**1.6**	**18.5**	**13.8**	**600**
[69]	ATF54143	2	<1	9.8	14.8	600
[70]	Philips-BFG425W	0.9	1.3	>20	15.8	200
[71]	MRF927T1	1	0.36	6	3.3	N/A
[72]	Infineon BFP420	1.9	1.5	>15	16	120
[73]	BJT-NPN	1	1.87	>20	14.3	N/A

Table 3.1: Reported LNA comparison around 2 GHz

transistors with similar characteristic values. All designs are below or around 2 GHz frequency range.

3.4 Conclusion

This work presents a wideband low-noise amplifier design procedure, simulation, and measurement results. The design utilizes distributed elements to realize input and output matching networks. Moreover, a passive DC bias network is used instead of an active DC bias network in order to have design simplicity. The lumped elements are not exploited due to the possible effect of parasitics on R-L-C components and to avoid the fabrication process errors.

The designed amplifier has 13.84 dB gain with ± 1 dB with about 600 MHz bandwidth. It has minimum noise figure of 1.615 dB, input return loss of -18.36 dB, and output return loss of - 7.89 dB. It is observed that Sonnet Software EM simulation and the measured results of the amplifier have a close correlation. As shown in table 3.1, comparison between mentioned studies and this work shows that the designed LNA has a wider bandwidth and a moderate gain with a low-noise figure and a good input return loss. Hence, it is a good alternative to the fourth generation (4G) LTE, Wi-Fi, and WiMAX applications.

CHAPTER 4
WIDEBAND BJT AMPLIFIER DESIGN WITH LOW VSWR AT 3 GHZ

4.1 Introduction

Bipolar junction transistor (BJT) can be useful for several wireless communication applications and they are one of the main components that affect the overall performance of the entire system. In order to achieve the desired performance, a transistor must be properly terminated at both its input and output ports. A design that includes both input and output matching networks is needed to terminate the transistor to the characteristic impedance of the system. Parameters that need to be taken into consideration when designing LNA are power gain, stability, noise figure, bandwidth, DC conditions, and VSWR.

In this work, the main goal is to have wideband, low noise figure, and low return loss. VSWR is a measure of the reflected power of the transmitted signal. In the same sense, return loss is the loss in the power of the transmitted signal. There has been many research related to wideband LNAs, however, this study focuses on the designs that are single-stage and utilizing microstrip technology.

In [84], a low noise amplifier operating over the frequency range of 3.5-4.5 GHz is

designed with the quality factor method. In this method, IMN and OMN are realized based on the Q-circles on the Smith Chart. Two different designs are introduced, however, for comparison, only a single-stage design is considered.

In [85], LNA design is based on QPSK modulation and channel modeling. The design is working at 2.3 GHz and achieving the noise figure of smaller than 1. However, bandwidth is considerably narrow.

[86] presents a single-stage LNA with BJT. The design is based on defining Γ_S and Γ_L in the noise figure circle. These results show that the design can give 10.1 gain with noise figure of smaller than 3.

In [87], highly linear LNA design with an on-chip transformer is presented. Even though results show that the gain is 33 dB, the system produces noise figure value greater than 2.

In [88], two amplifiers which operate at 1 GHz are presented with common emmitter and common base configurations. In order to achieve wider bandwidth, inductor and capacitor maximizing techniques are applied. Both amplifiers are designed to be used in an optical application.

An ultra-wideband (UWB) LNA design is described in [89]. This design is an example of inductive maximazing that uses multiple feedbacks. In the proposed method, LNA has two stages. At the base of the second stage transistor, an inductor is used in series. Measured results show that 5.7 dB of noise figure and 27 dB input return loss over the band of 3.1 - 10.6 GHz achieved.

In [90], a single-stage LNA design is illustrated. The methodology used in this design is to utilize the compact microstrip resonant cell (CMRC) at the emitter of BJT. This method yields to impedance bandwidth improvement and measurement results provides 1.5 dB noise figure and 15 dB gain over the frequency band.

Another wideband LNA example is described in [91]. The design uses cascode linked BJT to enhance noise figure. Experimental results show that the fabricated circuit yields

noise figure of 8.3 dB over the frequency band of 0.1 - 8 GHz.

4.2 Proposed Design

The design procedure starts with specifying: gain, bandwidth, noise figure, input, and output return loss. Once specified, Γ_S and Γ_L values need to be selected. Before choosing Γ_S and Γ_L, the transistor's input and output stability circles must be plotted to identify the available stable regions for the selection on the Smith chart. Then, the desired constant gain circles can be plotted to narrow down the Γ_S and Γ_L values needed to design the input and output matching networks.

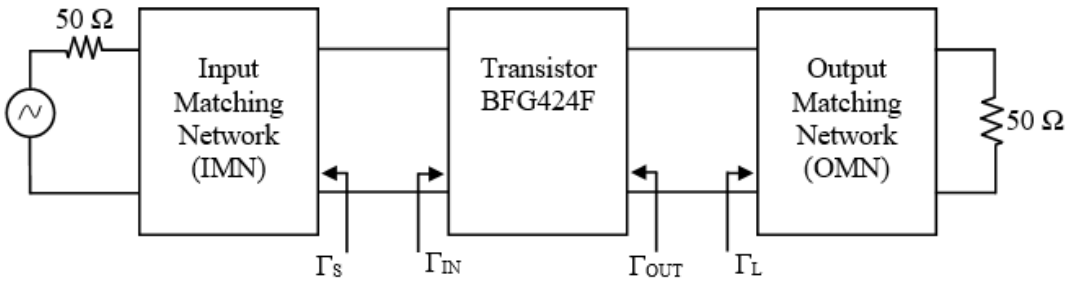
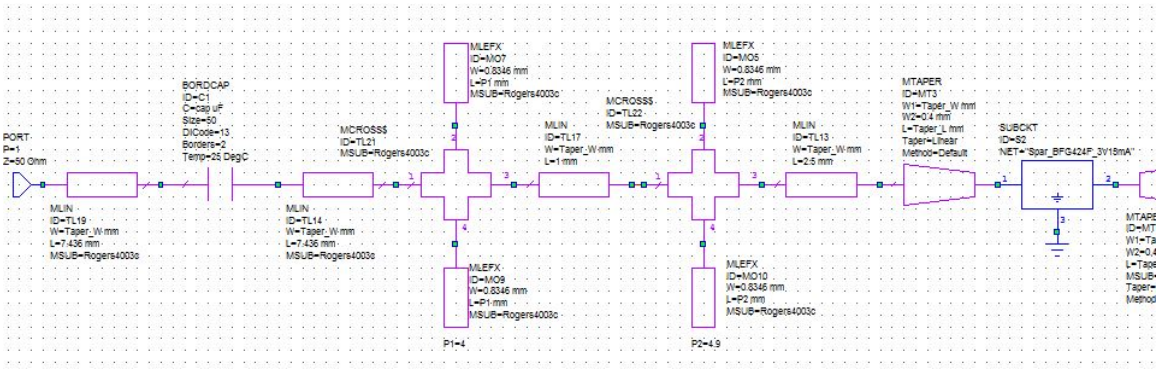


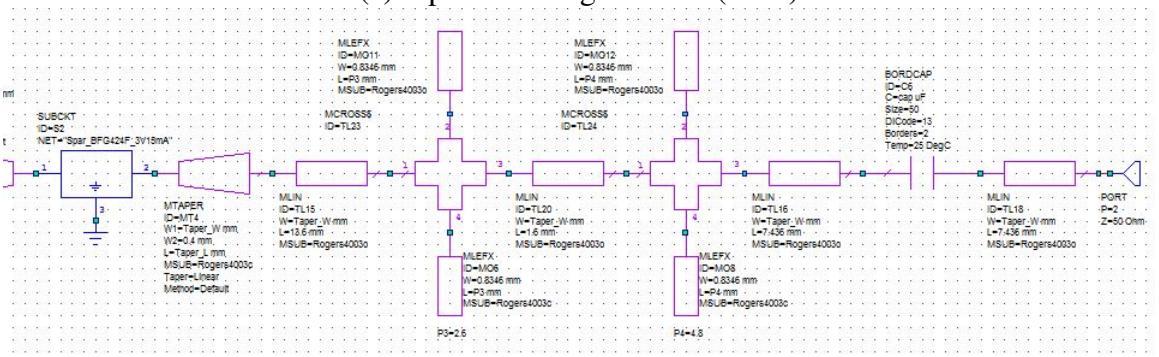
Fig. 4.1: LNA block diagram at 3 GHz

The design methodology in this work is based on using distributed elements for IMN and OMN while utilizing a passive DC bias network. Figure 4.1 shows a block diagram of a basic microwave amplifier.

The selected transistor was NXP's BFG424F [92]. The S-parameter data that is used throughout the design has bias conditions of $V_{CE} = 3V$ and $I_C = 15mA$. The selected board was Rogers 4003c, with a dielectric constant of ϵ_r = 3.55, a substrate thickness of 60 mils, and copper thickness of 0.669 mils. The initial design started with the simultaneous conjugate match for both the input and output matching networks at 3 GHz center frequency. The goal of ideal design was to get 12.5 dB gain, bandwidth of 300 MHz, and an input/output VSWR of less than 2. Additional design constraints were to use distributed



(a) Input matching network (IMN)



(b) Output matching network (OMN)

Fig. 4.2: Input matching circuit (a) and output matching circuit (b)

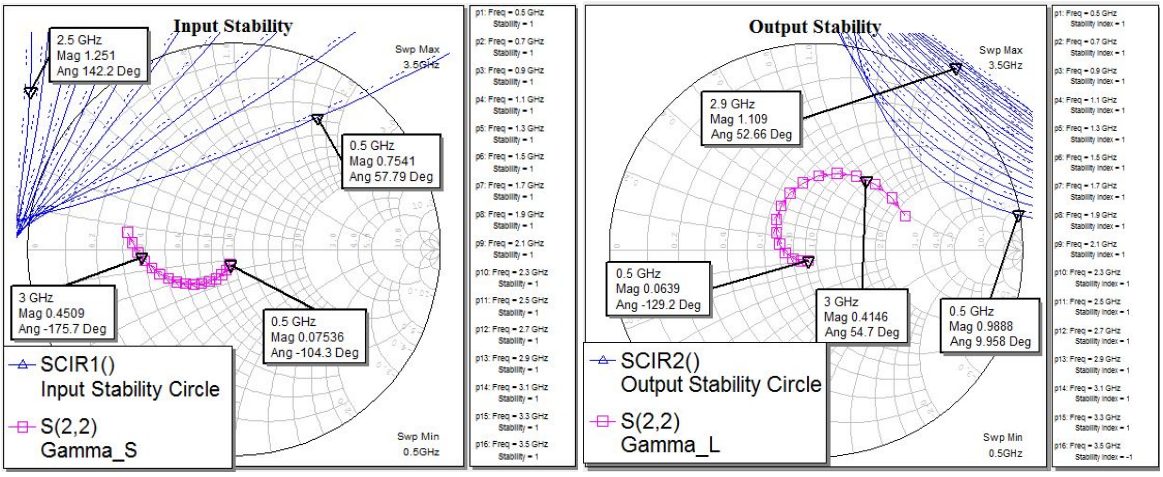
elements, to easily allow stub tuning after board fabrication.

A self-imposed design constraint was to use only open circuit stubs for the matching networks. This constraint ensured a lower occurrence of error by avoiding additional via effects. With the vias having non-zero resistance to the ground plane, new errors would have been accumulated. Additionally, if short circuit stubs were used, vias would not have been allowed to connect directly to the ends of the stubs, rather through a capacitor, and then to ground. The capacitor is needed to prevent the DC biases from being affected. Furthermore, with short circuited stubs, post fabrication tuning would not be as practical as it would be if open stub were used. Figures 4.2 (a) and 4.2 (b) show the complete schematic of the amplifier.

The input and output matching networks were designed based on the optimum Γ_S and Γ_L points, at 3 GHz, using double stub tuning. After the matching networks were designed for the optimal gain at 3 GHz, they were slightly modified to reduce the overall gain and

increase the bandwidth. With the use of Microwave Office Advance Wave Research (AWR) software, the lengths and placements of the ideal microstrip stubs were found. Initially, the microstrip stubs had a characteristic impedance of 50-Ohm at 3 GHz. However, when the desired stub lengths are selected, each single stub is converted into two 100-ohms stubs of equal length in order to balance the electromagnetic effects on the amplifier.

For DC blocking purposes, 2200 pF capacitors were used at both input and output ports, followed by a $\frac{1}{8}$ λ transmission line. Figure 4.3 shows that the designed Γ_S and Γ_L are in the stable region over the frequency range 0.5-4 GHz.



(a) (b)

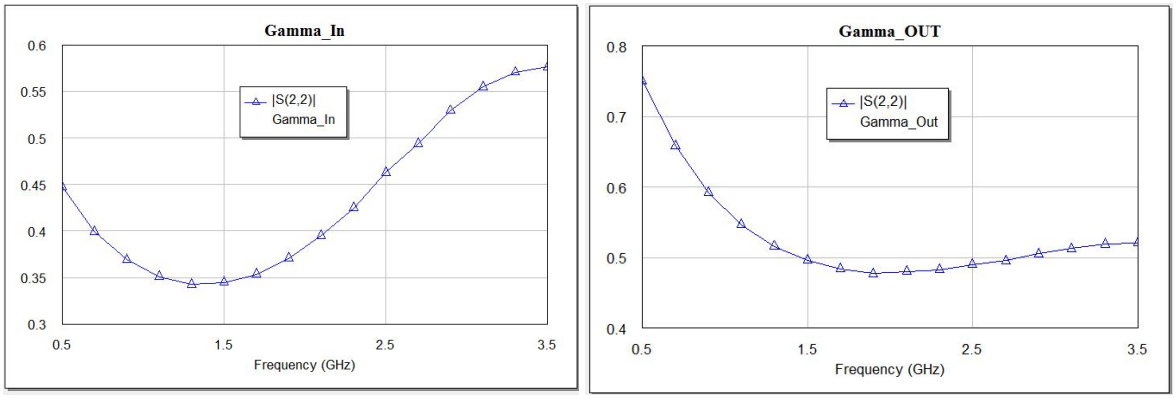
Fig. 4.3: Γ_S and Γ_L of the matching network

Figure 4.4 presents that Γ_{IN} and Γ_{OUT} have magnitudes of smaller than 1 which makes the design stable. Circuit simulations were run in AWR Design Environment.

Figure 4.5 shows the circuit simulation results of input and output voltage standing wave ratio. Both values are below 1.5 at the center frequency band.

4.3 Experimental Results

The next step in the design process is to perform an electromagnetic simulation of the amplifier by using appropriate software to see the complete board layout and any cross-



(a) (b)

Fig. 4.4: Γ_{In} and Γ_{Out} of overall amplifier

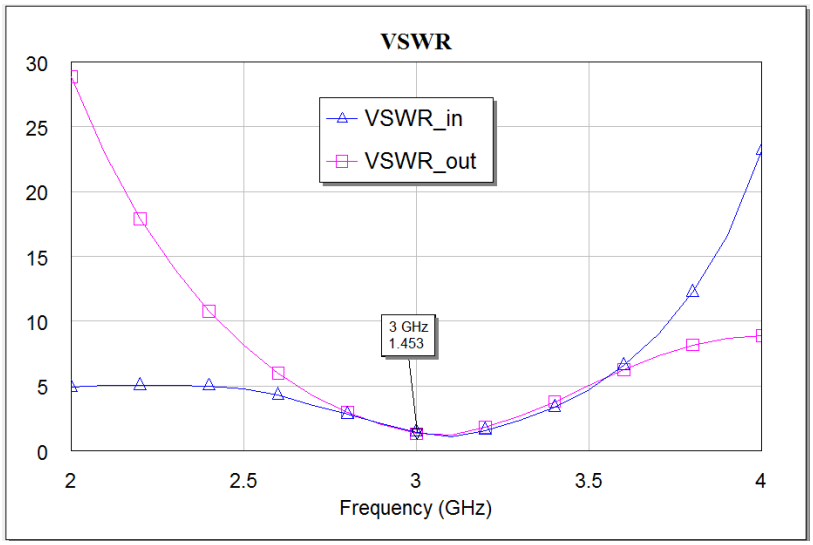
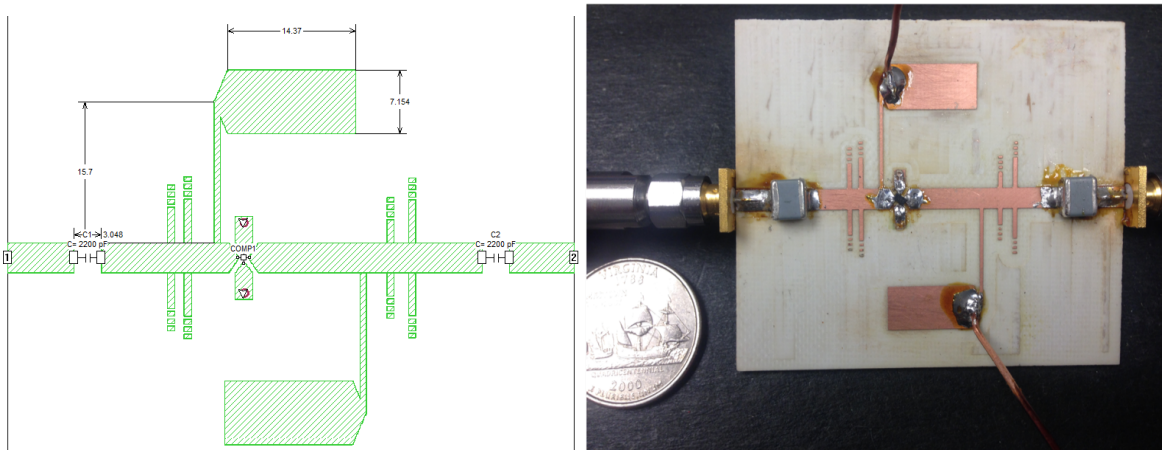


Fig. 4.5: Circuit simulation of input and output VSWR

coupling effect. Sonnet Software was chosen for this task because of its reliability and simplicity. To perform the Sonnet simulation, a layout DXF file can be exported from AWR and imported to Sonnet. Once imported, the physical effects of the placement of the stubs, microstrip junctions, transistor pad layouts, and via sizes should all be taken into account. Practical considerations that influenced the final layout of the board were rotating the transistor, adding tuning pads near the ends of the stubs, and selecting the connection locations of the RF chokes that lead to the DC power supplies. Originally, the plan was to have the input and output matching networks vertically offset from each other, thus allowing for the transistor to have a square alignment with the rest of the board.

The alternative, however, was to have the IMN and OMN vertically aligned and rotate the transistor by 45 degrees. By doing so, the transistor pad layout was symmetrical in both the horizontal and vertical directions.

At the ends of the open stubs, three empty pads were placed nearby. The empty pads allowed a place to add copper tape to extend the lengths of the stubs. It is known that simulated results do not guarantee perfect electromagnetic effects and all of the stubs and transmission lines are affected by the accuracy of the milling machine. To resolve some of the incurred errors by the milling machine, non-ideal vias, and non-homogeneous substrate structure, post fabrication tuning of the amplifier is needed. When deciding where to connect the DC bias transmission lines, an issue arises, which is that if they are connected in the wrong location, this might cause the amplifier to oscillate. Even though the DC bias transmission lines acted as an open circuit at the center frequency, the lines added unwanted reactance at the lower frequencies. One solution to this issue was to use a high impedance line that was $\frac{3}{4}$ λ long, rather than just $\frac{1}{4}$ λ long. This solution, however, was not implemented in the final design. Instead, a different DC pad layout was implemented that had a total electrical length of $\frac{1}{2}$ λ.



(a) Circuit Layout (b) Fabricated Circuit

Fig. 4.6: Low-Noise amplifier at 3 GHz

In this amplifier, a DC bias network was designed but not implemented because the DC voltages were supplied by two independent voltage sources. So instead of a DC bias

network, two low impedance pads, $\frac{1}{4}$ λ long, followed by high impedance lines, $\frac{1}{4}$ λ long in the shape of a flag, were added in Sonnet Software. In practice, the placement of the RF chokes to the DC pads should not be placed randomly, instead, they should be connected in a location that will have the least RF effect at the center frequency. In this design, the connection is made at the junction of the high impedance line and low impedance pads of the DC bias lines. At this junction, the amplifier sees an RF short, so anything in parallel with it would have no influence on the remainder of the circuit. Figure 4.6 presents the circuit layout and the fabricated circuit. Bias conditions for testing were $V_{CE} = 3V$ and

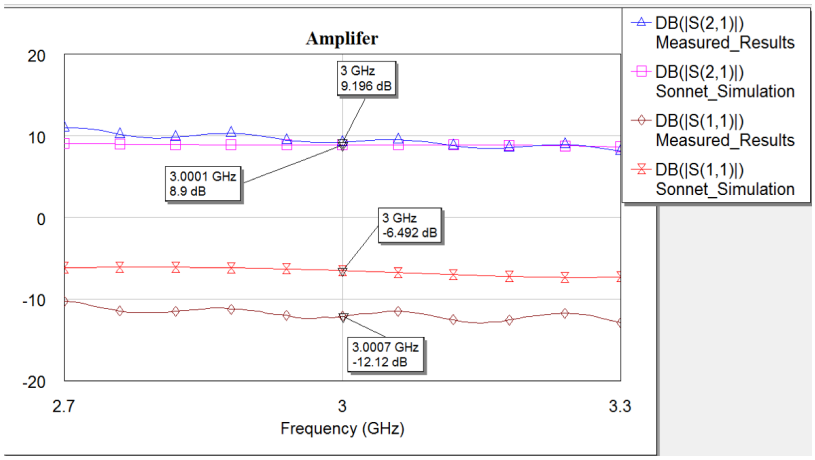


Fig. 4.7: EM simulated and measured S-parameters

$V_{BE} = 0.79V$. The transistor turns on at $V_{BE} = 0.7V$ if we are to achieve a larger gain as V_{BE} was increased to 0.79V. As shown in figure 4.7, the measured gain was 9.1dB. It shows a good agreement with the simulated result. Figure 4.8 shows the measured $VSWR_{in/out}$ over the band of interest. As shown in figure 4.8 specified $VSWR_{in}$ of smaller than 2 was achieved. $VSWR_{out}$ specifications were relaxed in order to meet other important parameter specifications, such as VSWRin and gain. Figure 4.9 provides the noise figure values of 1.5 at the center frequency. Over the operating band, the value is smaller than 1.7 which is expected based on the transistor's datasheet.

Figure 4.10 shows the measured result of two tone test. It illustrates the results for input power of -65 dBm, at this input power the third order intermodes are at the same level as

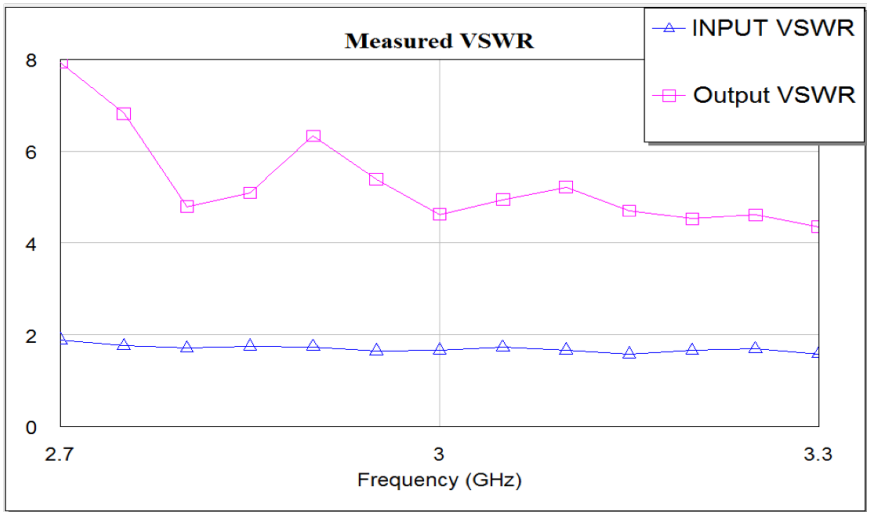


Fig. 4.8: Measured input and output VSWR

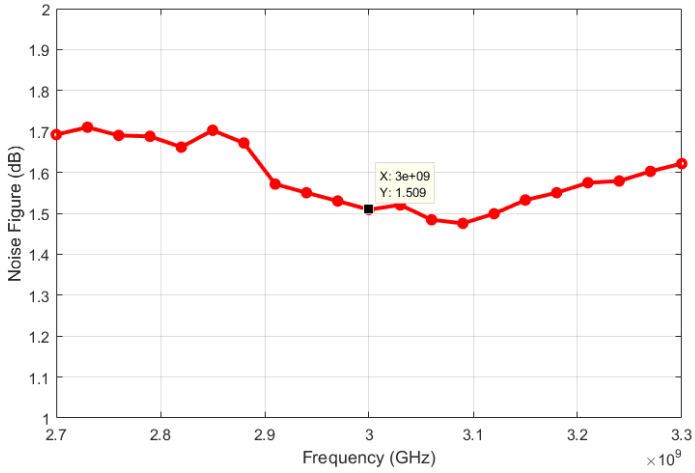


Fig. 4.9: Noise figure of the LNA

noise and no peaks for intermodes. Figure 4.11 presents the result for input power of -55 dBm, the third order intermodes are 25 dB which is below the two tones.

Table 4.1 shows the comparison between this work and the reported amplifier design with a similar transistor operating at L- and S-band frequency range.

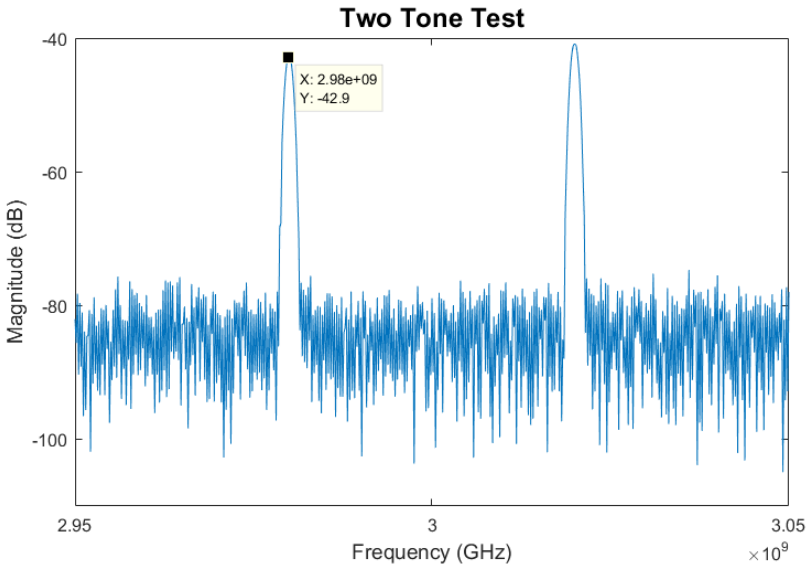


Fig. 4.10: Two-tone test

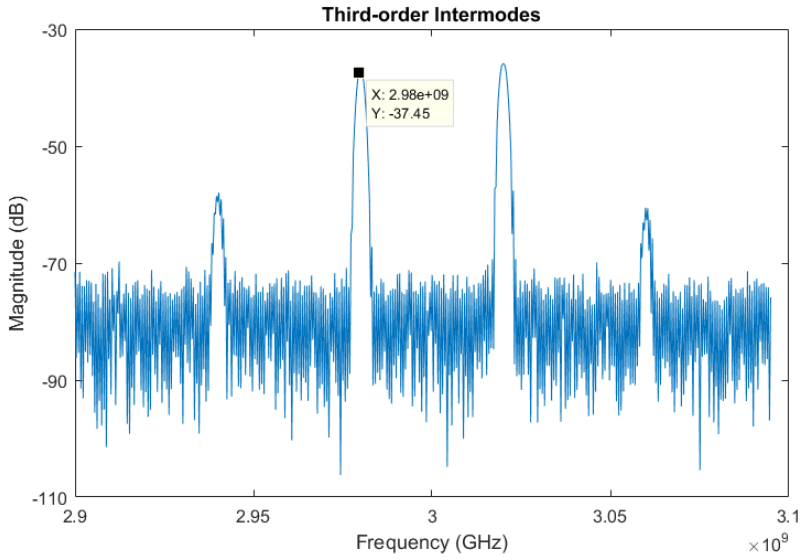


Fig. 4.11: Third-order intermodes

4.4 Conclusion

In this work, the design procedure of a microwave amplifier and an example of a BJT low noise amplifier operating at 3 GHz were studied. The design methodology is based on microstrip technology. Input and output matching networks are realized based on Γ_S and Γ_L points chosen from the transistor's available stabil regions. Lumped elements were

Reported Studies	Transistor Model	Frequency (GHz)	Noise Figure (dB)	Gain (dB)	VSWR	Bandwidth (GHz)
This work	**BFG424F**	**3**	**<2**	**11.81**	**<2**	**600**
[84]	ATF36077	4	<2	10.2	<2	550
[85]	ATF54143	2.3	<1	13	<3	20
[86]	SP-HP-AT-41511	2.4	<3	10.1	<2	400
[87]	On chip V-NPN	2.4	<5	33	<2	N/A

Table 4.1: Reported BJT amplifier design around 3 GHz

not used to design the networks due the complexity of the design fabrication process and possible parasitic effects of R-L-C components. Furthermore, the design of a DC bias network is completed in the same fashion and without using lumped elements.

The electromagnetic simulation and measured results were also compared. The simulated sonnet results more accurately represent the measured data. Although the amplifier was designed for a DC bias of V_{CE} = 3V, when the amplifier was tested, the measured results did not vary significantly when the V_{CE} bias was swept from 3V to 5V. After building the amplifier, additional factors need to be noted for the future amplifier design. First, it should be ensured that the transistor has a good ground connection by adding more vias to the grounding pads. Second, by using two independent sources for the DC biasing, the transistor can be easily burnt. Additionally, 50-ohm transmission lines should be connected to the transistor's legs, a tapered transmission line of a length of 1mm should be used.

By simulating different lengths of the tapered lines, drastic effects on the amplifier's performance are noticed, if the tapered lines were too long. Finally, through design procedure notes, it has been noted that if the tapers are long and the narrow ends are to be soldered to components, such as a transistor, the narrow pad will have a low structural durability. This low structural durability will have a huge effect when components need to be un-soldered and swapped out, thus running the risk of ripping off the pad. With that in mind, a short taper length should be kept.

While going through the design process, it was realized that when the bandwidth is increased and kept at a constant gain across that bandwidth, the VSWR also increased at

the lower end. This happens because the chosen transistor has a larger maximum stable gain at high frequencies than lower frequencies. Thus, to achieve a constant gain across the bandwidth, higher frequencies must have a closer conjugate match than lower frequencies. The more un-matched the lower frequencies get, the larger the VSWR becomes at those frequencies. Therefore, it would not be possible to achieve very large bandwidths without a second transistor and some wideband couplers.

Another design consideration that needs to be addressed is the via connections. Through measurements and comparisons with other researches, it became clear that the via placement, via size, and the number of vias cannot be neglected. On this design, two vias were used with diameters of 0.7 mm and one via for each emitter pin. The via pads had a simple rectangular geometry. With only two vias, the emitter pins did not have a good ground connection. To further reduce the via effects, it is recommended to use a thinner substrate. The DC resistance of the emitter grounding pads was measured at 5-ohm each. Because there were two pads, the total emitter to ground resistance was 2.5-ohm.

After connecting the DC bias pads, the amplifier had the potential to oscillate at 900MHz. In order to investigate this, the DC bias pads alone were simulated at 900 MHz and the pads acted like a short circuit. So, at the junction where the pads meet the input and output matching networks, the amplifier will see a short circuit in parallel with itself. Under certain conditions such as high VBE, the amplifier would oscillate. Therefore, when using the DC bias pads, they are only reliable at and near the center frequency. At lower or higher frequencies, the pads could potentially act like an RF short or RF open, thus making the design potentially unstable.

As a result, measured results prove that the designed amplifier has sufficient bandwidth with a low VSWR value and it would be an efficient low noise amplifier for the receiver side of the communication systems wireless application over the frequency band of 2.7- 3.3 GHz.

CHAPTER 5
A MODIFIED DOHERTY-LIKE AMPLIFIER DESIGN WITH A 10 W GaN TRANSISTOR

5.1 Introduction

In recent years, various DPA designs using different transistor technologies have been reported such as Gallium Nitride (GaN), Gallium Arsenide (GaAs) and Silicon Laterally Diffused Metal Oxide Semi-Conductor (Si-LDMOS). Most of these designs focus on efficiency enhancement, linearity, and bandwidth increase. In this study, the main focus is on the wideband single frequency and multi-band DPA with high efficiency and linearity using GaN devices.

Ever-evolving wireless communication systems require high data rate transmission. To achieve this, effective modulation schemes with high PAPR signals are needed. Therefore, PA designs with enhanced efficiency and high-power level are desired. DPA is a good candidate to overcome this problem. However, bandwidth limitation is a major disadvantage of DPAs. Theoretical and practical band limitations are explained in section 2.5.

Table 5.1: Broadband DPA Comparison

Refs.	**Year**	**Transistor**	**Freq. (GHz)**	**FBW (%)**	**Drain Eff. (%)**	**OBO Power (dB)**	**Psat (dBm)**	**Gain (dB)**
[93]	2012	CGH40010	3-3.6	18	38	6	43	∼10
[94]	2012	CGH40006P	2.4-2.9	19.2	40	6	35	∼7
[95]	2012	CGH40010	1.96-2.46	23	40	6	N/A	∼7
[96]	2013	CGH40010\ CGH40025F	1.7-2.8	50	47	6	44	∼13
[97]	2013	CGH60015DE	1.5-2.4	45	49	6	36	∼11
[98]	2014	Gan Package	0.7-0.95	30	42	9	33.5	∼15
[99]	2014	CGH40010	0.8-1.2	40	50-70	9	N/A	>10.8
[100]	2014	CGH35015	1.6-3.3	65	N/A	6	N/A	12.3
[101]	2015	CGH27015	1.7-2.75	47	37-48	6	N/A	>8.5
[102]	2016	CGH40010	1.65-2.75	50	52-66	6	44.5-46.3	10.5
[103]	2017	MGFS39G38L2	3-3.6	18	46	>7	N/A	12
[104]	2018	CGH40010	1.5-3.8	87	33-55	6	42.8	11.9
[105]	2018	CGH40010	1.5-2.6	53.6	31-35	6	35	20
[106]	2018	CGH40045	1.5-2.5	50	43	6	45-47	N/A
[107]	2019	CGH40010	1.6-2.6	47	53-66	6	45.6-46	8.6
[108]	2019	CGH40010	1.4-2.1	40	60-65	6	42.8-43.5	9.4

Most of the reported DPAs work with narrow band. Load modulation and quarter-wave impedance inverter are some of the factors for having a narrow operating frequency band of DPAs. Additionally, harmonic terminations and impedance matching at different power levels need to be taken into considerations. There are several research regarding the enhancement methods of bandwidth on DPAs [93–108]. Table 5.1 shows comparison between selected studies.

In [93], the authors proposed a method that exploits an output compensation network at the output of main and peak amplifiers while implementing second harmonic tuning at the main amplifier, which leads to gain improvement over the frequency band. Proposed method utilizes a 10-W GaN HEMT on SiC transistor from Cree with 28 volt drain bias. The design provides 38% efficiency and saturated power of 43 dBm with 18% fractional bandwidth (BW) at 6 dB output back-off power. Fabricated circuit operates between 3 - 3.6 GHz with 10 dB gain.

In [94], the real frequency technique is introduced to have optimum impedance matching. Theoretical proof of the design is drawn and the suggested method is implemented using a 6-W GaN transistor from Cree. Measured results show 19.2% BW with 40% drain efficiency at 6 dB OBO power. The desing works over the frequency band of 2.4 - 2.9 GHz with 35 dBm saturated power and 7 dB gain.

In [95], modified DPA architecture is proposed. The design eliminates the quarterwave impedance inverter to obtain broader bandwidth. Theoretical analysis to find optimum load impedances to design output matching networks are derived. The proposed design theory is validated by fabricating a 10-W PA with a GaN transistor. IMN and OMN are realized using only lumped elements. Measured results show provide 40% drain efficiency with 23% bandwidth.

In [96], the same method is applied as in [95]. However, in this case different transistors are used for main and peak amplifiers. For proof of concept, a DPA is designed with a 10-W GaN (CGH40010F) for main amplifier and a 25-W GaN (CGH40025F) for peak amplifier. Results provides 50% BW and 47% drain efficiency with saturated output of 44 dBm at 6 dB OBO power. The design brings 13 dB gain between 1.7 - 2.8 GHz.

In [97], individually controlled dual RF input was proposed. Theoretical proof shows that proposed method can provide high efficiency at output back-off power and output power. Sample circuit was designed using 15-W GaN HEMT transistor from Cree. Results show that higher efficiency and wider bandwidth were obtained comparing to conventional DPA. The design was able to achieve 45% BW, 49% drain efficiency and 36 dBm saturated output power. Additionally, circuit provides 11 dB gain between 1.5 - 2.4 GHz.

In [98], the proposed circuitry introduces lump element (LC) network at the output side of the peak amplifier. LC tank operates at the center frequency and act like an open circuit. At the second harmonic, it behaves as short circuit, thus main amplifer works as Class F amplifier and achieves wider bandwidth. In order to demonstrate the concept, asymmetrical DPA was designed using 10-W and 25-W GaN HEMT. Results show 30% BW and 42 %

drain efficiency at the 9 dB OBO. The sample circuit work from 0.7 GHz to 0.95 GHz with 15 dB gain and 33.5 dBm saturated power.

In [99], a modified DPA is designed without quarter-wave impedance inverter. The design uses 10-W GaN package transistors and provides high saturated output power of 40 dBm and 41% drain efficiency at the 9 dB OBO power between 2.45 - 2.8GHz. The fractional bandwidth is 15.4% and the gain is 8 dB.

In [100], this work presents a three-stage Wilkinson power divider in the input side and utilizes Klopfenstein taper to match the output of the main amplifier to the load. Measured results illustrates that the design achieves 65% fractional BW and 50% PAE.

In [101], the proposed design is an another example of Klopfenstein taper utilization. Additionally, the design uses asymmetrical single stage Wilkinson power divider. Fabricated circuit using 15-W GaN transistor and operating between 1.7 - 2.75 GHz. Results provide 47% fractional BW and drain efficiency better than 37% while obtaining gain better than 8.5 dB.

In [102] continuous mode technique is applied. To elaborate, isolation between main and peak amplifiers is necessary to avoid modulation at harmonic frequencies. In this case, modulation was intentionally allowed which leads to a wideband DPA. To validate the proposed idea, 13 W GaN HEMT from Cree used for the design. Test results present 50% fractional BW, 52-66% drain efficiency and 10 dB gain over the frequency band of 1.65 - 2.75 GHz.

In [103], a frequency dependent compensating network is designed. Additionally, a quarter-wave impedance inverter network using parasitic components were utilized. To justify the method, two-way DPA was designed using Mitsubishi GaN HEMT package transistor at the center frequency of 3.3 GHz. Test results show 46% drain efficiency and 12 dB gain.

In [104], the authors reported design of inverter network impedance which is calculated by the power devices' capacitance network which help proper impedance matching and

lead to 87% fractional bandwith, 42.8 dBm saturated power and 12 dB gain. The fabricated circuit uses 10-W GaN transistor and operates between 1.5 - 3.8 GHz.

In [105], dual-stage DPA uses a driver amplifier. Additionally, Klopfenstein taper is employed at the output side of the main and peak amplifiers to improve the bandwidth. The example circuit uses a 10-W GaN transistor. Measurement results provide 31% drain efficiency, 35 dBm saturated power, and 20 dB gain over the frequency band of 1.5 - 2.6 GHz with 53.6 % bandwidth.

Using complex-value load modulation to design output combining network, which leads to improved linearity and enhanced bandwidth reported in [106]. The proposed design utilizes 45-W GaN transistor and operates at the center frequency of 2 GHz with 50% bandwidth. At the 6 dB OBO, the design has 43% efficiency and 46 dBm saturated power.

In [107], the proposed method had three-stage with impedance compensating circuit. For peak amplifiers, dual-matching newtworks designed to optimize the impedance matching and this approach leads to an extension with the bandwidth. The fabricated circuit works over the frequency band of 1.6 - 2.6 GHz with 47% bandwidth. The design gives 53% efficiency, 46 dBm saturated power and 8.6 dB gain.

In [108], π-type harmonic injection network (HIN) was utilized to have second harmonic between main and peak amplifier. This caused bandwidth reduction because of frequency mismatch. In order to compansete this matter, impedance of the peak amplifer was decrased. This resulted in 40% fractional bandwidth with 60% drain efficieny. 43.5 dBm saturated power and 9.4 dB gain is obtained over the frequency band of 1.4 - 2.1 GHz.

Multi-band DPAs are needed to overcome the complexity of wireless communication systems as they can lead to size reduction and cost efficiency in circuits. Moreover, the devices that cover two or more bands are needed because the frequency spectrum is overutilized. Therefore, in order to design dual/multi-band operating devices, passive network architectures need to be analyzed. These architectures such as input and output matching networks, combining network, and phase delay line are important because they have

frequency-dependent characteristics.

New methods to have multi-band operating DPAs over different frequency range are reported in recent years [109–115]. Table 5.2 provides performance of the multi-band DPAs that are mentioned.

Table 5.2: Dual-/Multi-Band DPA Comparison

Refs.	**Year**	**Transistor**	**Freq. Range (GHz)**	**Drain Eff. (%)**	**OBO Power (dB)**	**Psat (dBm)**	**ACHL (dBc)**
[109]	2012	*CGH60015DE*	1.8/2.4	69-61	6	43	48-46
[110]	2013	*Not Specified*	0.9/1.5/2.1/2.6	58/60/52/43	6	48/56/47/32	N/A
[111]	2015	*CGH40010F*	1.6 /1.9 /2.2	46 /40 /42	6	N/A	N/A
[112]	2017	*CGH40010F*	1.82/2.1	49/44	6-\9	42.4/43/2	>18
[113]	2018	*CGHV1F006S*	1.8/3.8	38/52	8	37.4/45.4	51
[114]	2019	*CGHV1F40025*	2.1/3.45	48-43	9	48-47.5	45.9-47.3
[115]	2019	*CG2H40010*	1.42/2.4	61-52.8	6	43.5-43.6	26.2-26.5

In [109], passive RF networks were utilized to achieve dual-band. In proposed method, load-pull technique was exploited with second harmonic in order to have better efficiency. 15-W GaN transistor used in the design and the fabricated circuit provides two center frequencies, 1.8 and 2.4 GHz. At 6 dB OBO power, the design shows better than 61% efficiency and 43 dBm saturated power.

In [110], the design introduces quad-band impedance inverting network to provide good impedance matching. In order to achieve second efficiency peak at 6 dB OBO, proposed design used asymmetric drive powers of 10 W and 25 W for main and peak amplifiers, respectively. Although this reduced the gain, the design maintained better than 10 dB gain over the bandwitdh. This method was previously used for tri-band DPA design with different frequencies by the same authors in [116]. Measurement results show that the proposed design can have minimum 43% and maximum 60% efficiency.

In [111], design of a multi-band impedance inverting networks and phase offset lines were realized to achieve tri- and quad-band DPA. Proof of concept uses 10-W GaN transistor and shows that the design provided minimum of 30% and maximum of 46% efficiency

overall bands. This method prevously used by the same authors for dual-band application in [117].

In [112], reconfigurable dual-band DPA with 10-W GaN transistor was proposed. In this work, Impedance transformer utilizes series transmission line which has reconfigurable loading stubs. Experimental results show that minimum saturated power of 42.4 dBm and 44% efficiency.

In [113], peak amplifier was replaced by N number of peak amplifiers that were connected to impedance inverting network with N-1 section combiner. Same method was applied in [118] with differenct frequency bands. Dual-band circuit performs mininum of 38% and maximum 52% efficiency.

In [114], theoritical explanation of dual-band inverting networks which eleminates output capacitance of the transistors, was given. Proof of concept was built with 25-W GaN transistor and able to achieve 43% or better drain efficiency 47.5 dBm or better saturated power in both bands for this three way DPA.

In [115], dual-band impedance inverter was used to increase the performance of the DPA. Microstrip and coupled lines are utilized to in IMN and OMN networks. The proposed design utilized 10-W GaN transistor and the measured results illustrate 52.8% or better efficiecny and 43.5 dBm or better saturated power.

5.2 Proposed Design

Doherty Power amplifier design requires delicate attention as it is a challenging task to take care of different parameters at the same time. The low input power and high input power conditions of the conventional DPA is explained in section 2.5. DPA uses a quarter-wave impedance inverter to have load modulation for the main amplifier as it has different impedances based on the input power level.

At the low input power, peak amplifier is not turned on therefore it is seen as open. In

this case, the impedance seen by the main amplifier is 100 ohm. Thus, 50 ohm quarter wavelegth transmission line inverts 100 ohm to 25 ohm (see Figure 5.1). When the main amplifier reaches its saturation point, the peak amplifier becomes active and the system goes into high input power mode. In this case, the impedance seen by the main amplifier is 50 ohm while the impedance seen by the peak amplifier is 50 ohm (see Figure 5.2). Therefore, the impedance at the connection point of the main and peak amplifier will be 25 ohm for both input power levels.

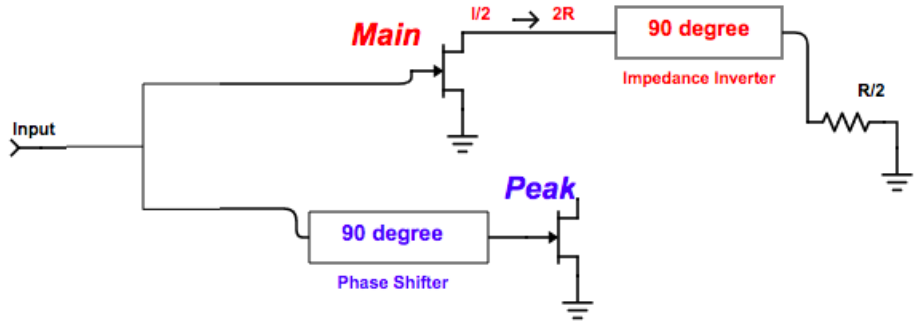


Fig. 5.1: Equivalent circuit diagram for low power region.

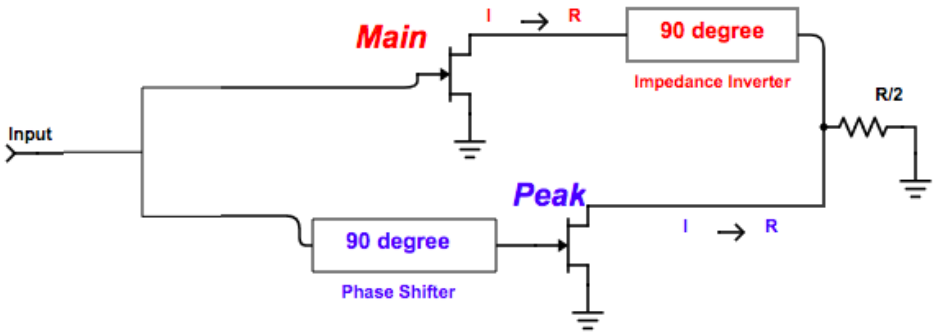


Fig. 5.2: Equivalent circuit diagram for medium power region.

This is how the DPA works in theory, however, it has practical drawbacks. In this case, impedance inverted at the output of the amplifier. This load modulation may not be optimum because of transistors' nonlinear behavior [49]. The output matching network of the main amplifier should be taken into consideration, as well. Moreover, matching the outputs of the amplifiers to two different impedances using a quarter wavelength transmission line limits the bandwidth due to the frequency response of the quarter-wave transmission line.

In this proposed design, the goal is to eliminate the quarter wave impedance inverter at the output side of the amplifier and to find the optimum load impedances to realize the OMN. Moreover, while designing the IMN and OMN considerations are to use only distributed elements and to utilize tapered line. Designing the OMNs has an important role on the overall performance of the amplifier. The aim in this design is to achieve maximum PAE and the peak output power. In order to meet the aim, optimum load impedances need to be defined by load-pull simulation from the transistor's large signal model provided by the vendor.

The proposed design theory for this study is based on the research introduced in [95]. In [95], the authors validated the design with a 10-W amplifier using GaN transistor. In the mentioned design, quarter-wave impedance inverter eliminated as well as the off-set lines at output of the main and peak amplifiers. The design uses only lumped elements for the matching circuits. At the input section, a single stage equal power splitter is utilized. Based on this theory, there are other studies to increase bandwidth. In [99], the authors avoid using impedance inverter, however, offset lines at the output matching networks of the main and peak amplifier are used. Also, the design uses distributed elements instead of lumped elements. In [100], the authors use a three-stage equal split Wilkinson PD and delay line at the input side. At the output side, tapered line impedance inverter is utilized only in the main amplifier's output to achieve broader bandwidth. Similarly, in [101], tapered line impedance inverter used with un-equal single-stage Wilkinson PD. All these mentioned studies eliminates or modifies the impedance inverter to achieve broader bandwidth.

The design flow of conventional PA is presented in section 2.2 and it consists of several steps. The first step is to determine the specification of the DPA. The goal is to design an amplifier which operates at 2 GHz center frequency and provides 15 dB gain, 39 dBm output power, and 45% power added efficiency (PAE) at the 6 dB output back-off power (OBO).

The second step is to select the active device, transistor. The selected transistor is 10-

W GaN from Cree with the model number of CGH40010 [119]. The bias condition for the selected device is V_{DS} = 28 V and I_D = 200 mA. The selected substrate is Rogers' RO4003C with a dielectric constant of ϵ_r = 3.55 and substrate thickness of 60-mil with 0.5 oz copper thickness [81].

Rest of the steps consist of load-pull and source-pull simulations, power divider design, input and output matching network design for main and peak amplifiers. These steps will be explained in the following subsections.

5.2.1 Load Pull and Source Pull Simulation

One of the important steps in designing a PA is load-pull/source-pull simulation. It helps to determine the load and source impedances and provides information about several parameters such as output power, efficiency, and gain that might be obtained from a transistor.

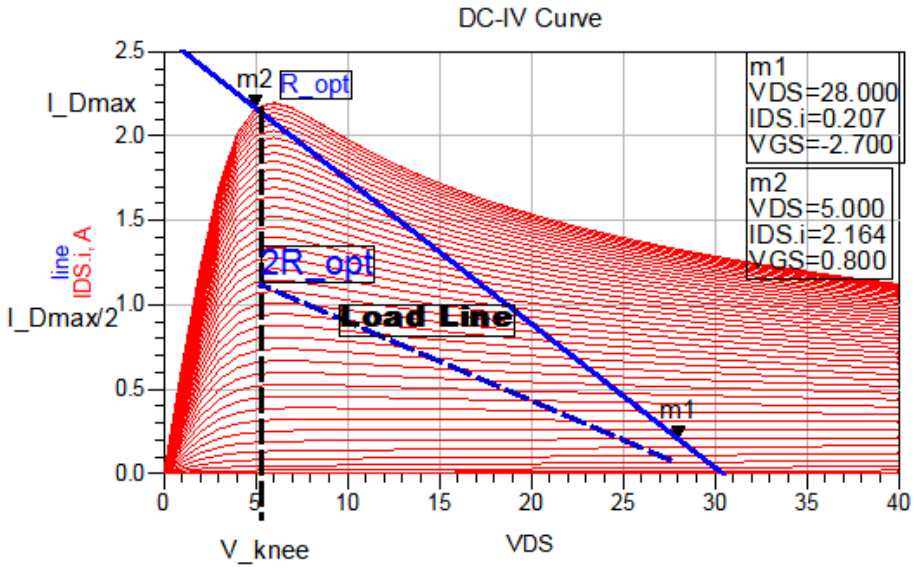


Fig. 5.3: DC-IV curve of the selected transistor

In the load-pull simulation, the goal is to find the optimum load impedance which will be presented to a device. Nonlinear device model is plotted on a Smith chart with contours of constant performance. From the load-pull contours and data, it can be seen what impedance to present to your device and what performance you can expect. The power

delivered to the load depends on the load impedance.

Large signal device model of the transistor is acquired from the vendor and processed with both AWR [79] and Advanced Design System (ADS) [120]. Figure 5.3 shows transistor's DC-IV curves with a DC bias point of V_{DS} = 28 V and I_D = 200 mA. This figure proves that the transistor turns on properly under the essential operating conditions. Blue line represent the load line of the transistor. The load line calculation formulas are the following:

$$P_{load} = \frac{1}{2} * V_{load} * I_{load} \tag{5.1}$$

where,

$$I_{load} = \frac{V_{load}}{R_{load}} \tag{5.2}$$

Therefore, P_{load} is equal to the following formula.

$$P_{load} = \frac{V_{load}^2}{2 * R_{load}} \tag{5.3}$$

Also, the slope of the load line can be written by the following expression.

$$Slope = \frac{1}{R_{load}} \tag{5.4}$$

When the input signal is low, the transistor conducts less current than the DC bias current. Therefore, the AC component tries to flow into the load. On the other hand, when the input signal is high, the transistor tends to conduct more current than the DC bias current, thus the AC component wants to flow away from the load. At low frequencies, where parasitic effects can be neglected, the power delivered to the load for a given bias point and input signal amplitude depends on the load resistance.

Figure 5.4 illustrates the time domain drain voltage and current measurements. Intrinsic voltage and current ports are provided by the vendor to measure voltage and current wave-

forms at the current generator of the transistor. Both voltage and current waveforms are plotted at the center frequency and available input power source of 32 dBm. Here, voltage minimums are closer to zero which represents the true intrinsic waveform.

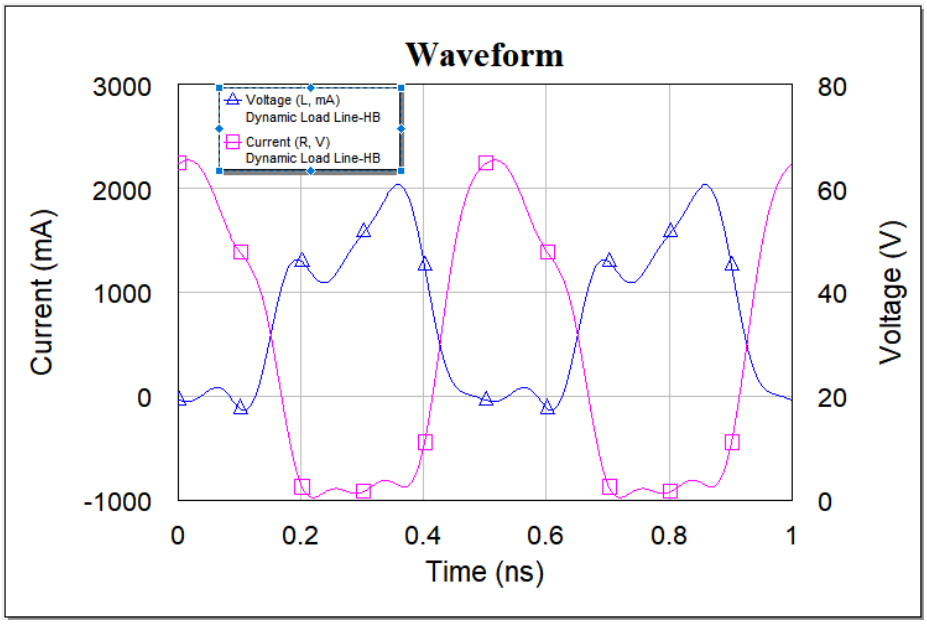


Fig. 5.4: Time domain waveform of the selected transistor.

In order to achieve the peak power delivered to the load, large swings in both voltage and current about the bias point is required. If the load resistance is too low, the current swing reaches its limits while the voltage swing is low. Thus, the power delivered is lower than it could be. If the load resistance is to high, the voltage swing reaches its limits while the current swing is low. So, the power delivered is lower than it could be. You want a load that enables both high voltage and current swings. While contours at low frequency appears both imaginary and real axis of the Smith chart. At RF and microwave frequencies, parasitic effects become significant and the optimal load moves off the real axis.

When setting for load-pull, the first step is to determine the range of load impedances to sweep or pull. Moreover, the bias voltages which will determine the bias current and the source impedance need to be specified.

Figure 5.5 shows the load/source-pull setup. After defining the bias voltages of the selected transistor, load-pull setup is used from the simulation tool. Here, parameters such

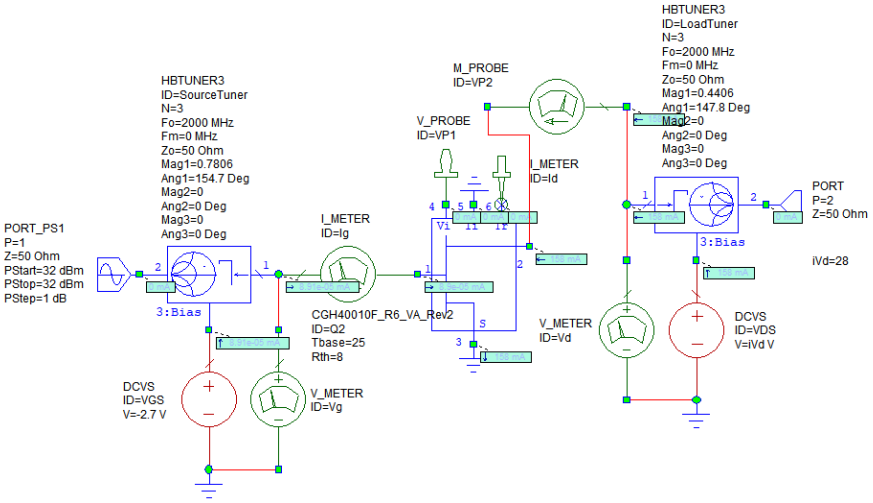


Fig. 5.5: Load/source pull setup.

as, input power source, gate, and drain voltages are entered based on the decided values. Several iterations might be necessary to make about the source and load impedances.

Figure 5.6 shows the source-pull contours and the maximum point for the power gain of the selected transistor. Optimum power gain point is selected to design input matching network. Simulation result show that the maximum power gain that the transistor can provide is 21 dB at the center frequency. Thus, Z_S is selected as 4.13 + j11.04.

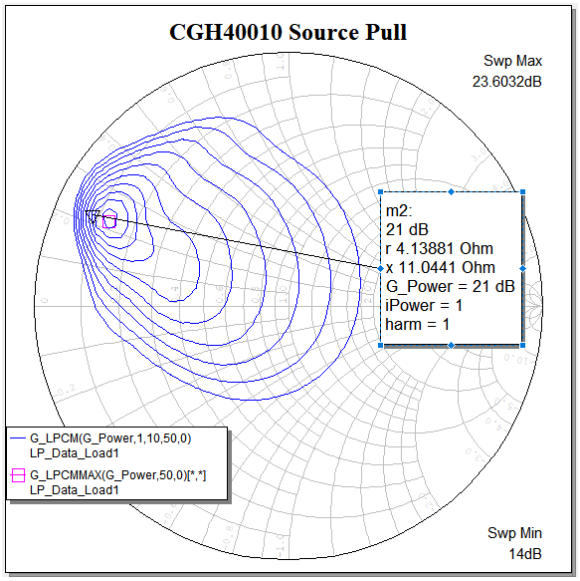


Fig. 5.6: Load pull contours of the selected transistor at 2 GHz.

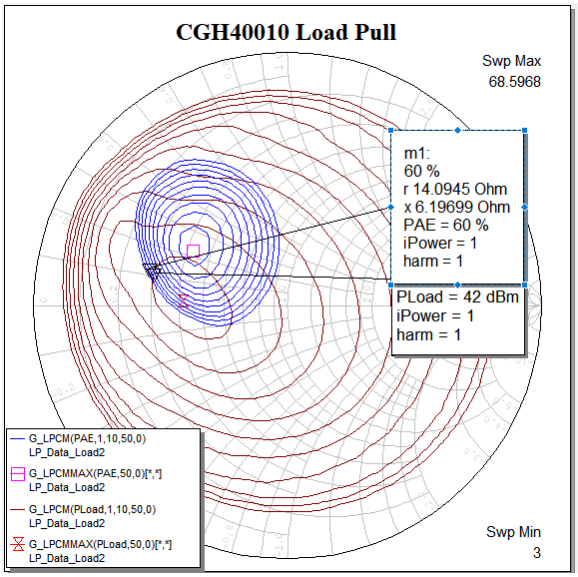


Fig. 5.7: Load pull contours of the selected transistor at 2 GHz.

Figure 5.7 presents the load-pull contours of the selected transistor at 2 GHz. Selected load impedances are midpoint between the maximum delivered output power and the peak power added efficiency for a V_{GS} such that V_{DS} = 28 V and I_D = 200 mA. Therefore, impedance point to design output matching network design is Z_L = 14.09 + j6.19. Based on the load-pull simulation result, the transistor can provide 42 dBm output power and 60% PAE. The next step is to design input power divider and then matching networks.

5.2.2 Power Divider Design

The Wilkinson Power Divider (WPD) was introduced by Ernest Wilkinson around mid-1960's. It is a three port network device which utilizes quarter wave transmission lines.

Mostly, it is used for equal split of 3 dB, however, arbitrary power division can be achieved, as well. When the output ports are matched properly, it will provide a lossless network. Also, it can be used as a power combiner. In this study, it will be used for equal power split and will be placed before the input matching networks of the main and peak amplifiers.

Figure 5.8 shows a three port ideal Wilkinson power divider diagram. The power di-

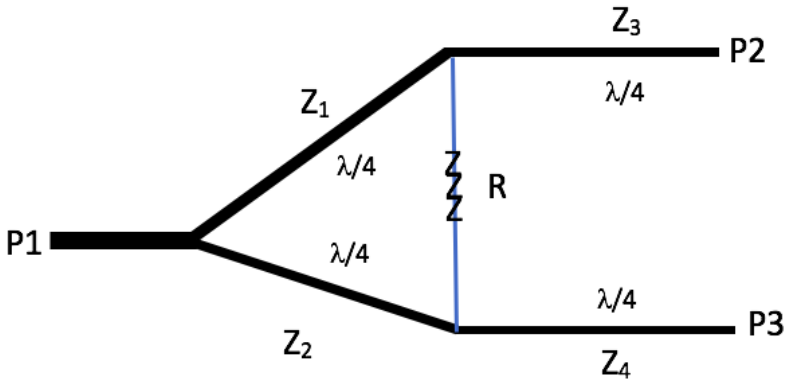


Fig. 5.8: Wilkinson Power Divider Diagram.

vider consists of two quarter wave length transmission lines with characteristic impedances of $\sqrt{2}Z_0$, two quarter wave length transmission lines with characteristic impedances of Z_0, and a resistor with the value of $2Z_0$ where Z_0 is 50-ohm.

In order to have sufficient reflection at each port and a good isolation between port 2 and port 3, characteristic impedances of quarter wave length lines need to be used as given above. These values can be optimized based on the simulation results. Here, theoretical calculations for the transmission lines and the resistor values can be derived from the following equations.

$$Z_1 = Z_0 \left(\left(\frac{P_2}{P_3} \right)^{-1.5} + \left(\frac{P_2}{P_3} \right)^{-0.5} \right)^{0.5} \tag{5.5}$$

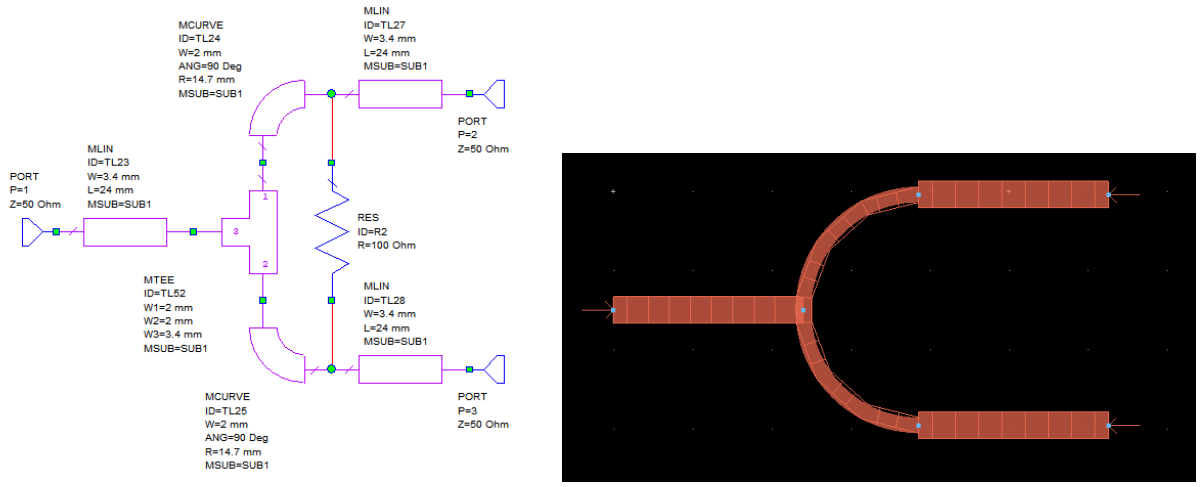
$$Z_2 = Z_0 \left(\left(1 + \frac{P_2}{P_3} \right)^{-1.5} \left(\frac{P_2}{P_3} \right)^{-0.5} \right)^{0.5} \tag{5.6}$$

$$Z_3 = Z_0 \left(\frac{P_2}{P_3} \right)^{-0.25} \tag{5.7}$$

$$Z_4 = \left(\frac{P_2}{P_3} \right)^{0.25} \tag{5.8}$$

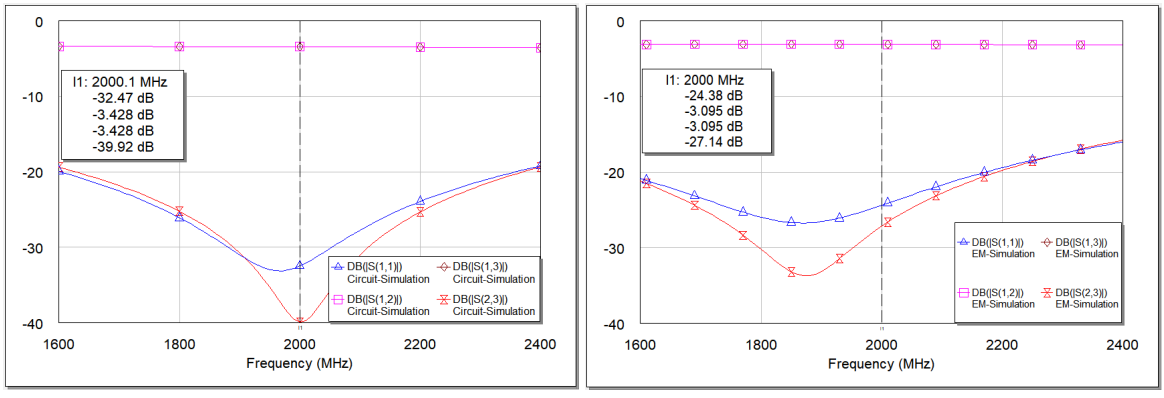
$$R = Z_0 \left(\left(\frac{P_2}{P_3} \right)^{0.5} + \left(\frac{P_2}{P_3} \right)^{-0.5} \right) \tag{5.9}$$

Initial impedance values of the quarter wave lines are 70.7-ohm for Z_1 and Z_2, 50-ohm for Z_3 and Z_4. Also, the resistor value is 100-ohm which ensures a good isolation between port 2 and port 3. Figures 5.9(a) and (b) show the circuit schematic and the layout of the WPD designed to operate at 2 GHz.



(a) Circuit Schematic (b) Layout

Fig. 5.9: Wilkinson Power Divider at 2 GHz.



(a) Circuit simulation (b) EM simulation

Fig. 5.10: Wilkinson Power Divider simulation results.

As seen from Figure 5.10, circuit and EM simulation results provide sufficient performance. Even though there is a slight degradation with the EM simulation, the return loss

value is better than -15 dB. Also, isolation between port 2 and port 3 better than -24 dB across the frequency band. Moreover, equal split values of 3 dB is achieved.

In this study, the Wilkinson PD is selected for a equal power splitter as it has simple structure and can be used with microstrip and striplines. Moreover, it provides high isolation between the output ports.

5.2.3 DC Bias Network

The goal of designing DC bias network is to define optimum quiescent of the transistor. Thus, the transistor can be in the active mode and might have limited voltage changes.

In this DPA configuration, the gate and drain of the transistor requires biasing network. Therefore, there will be two bias network design for each amplifier.

At the gate of the transistor, RF choke is used to short-circuit of the DC power. For this purpose, a quarter wavelength transmission line is preferred in general. At the drain side of the transistor, RF chose is used so that microwave frequencies seen as open-circuit. Other than the transmission lines, series resistors and parallel inductors and capacitors used to provide smooth transition.

5.2.4 Design of Input and Output Matching Networks

After completing the power divider design and achieved sufficient results, the next step is to design input and output matching networks for the main and peak amplifiers. The matching networks are required at the input and output of any amplifier structure to ensure smooth load transformation between the transistor's input and output impedances and the system impedance of 50-ohm. Conventional Doherty architecture has the same input and output matching networks for both main and peak amplifiers. Therefore, this section will cover matching networks for both amplifiers. Only difference between the main and peak amplifier is gate voltages. This is because the main amplifier is biased as Class AB and gate voltage is V_{GS}= -2.7 V. The peak amplifier is biased a Class C and the gate voltage is

V_{GS}= -4.7 V.

In section 5.2.1, the optimum source and load impedances are determined by the source and load pull analysis of the transistor. The selected Z_S and Z_L are 4.13 + j11.04 and 14.09 + j6.19 respectively. These values are then used in Smith chart matching tool in the ADS as the starting points.

The input matching circuit is designed with distributed elements only. The initial design started with the simultaneous conjugate match for the source impedance at the center frequency of 2 GHz. Then, the length and width of the transmission lines are realized and optimized in the simulation tool. The input matching network includes two open-stubs. The second open-stub which is closer to the gate of the transistor is later divided into two equal length to shorten the length of the transmission line. Additionally, on the peak amplifier's input matching circuit, a piece of transmission line added for phase compensation.

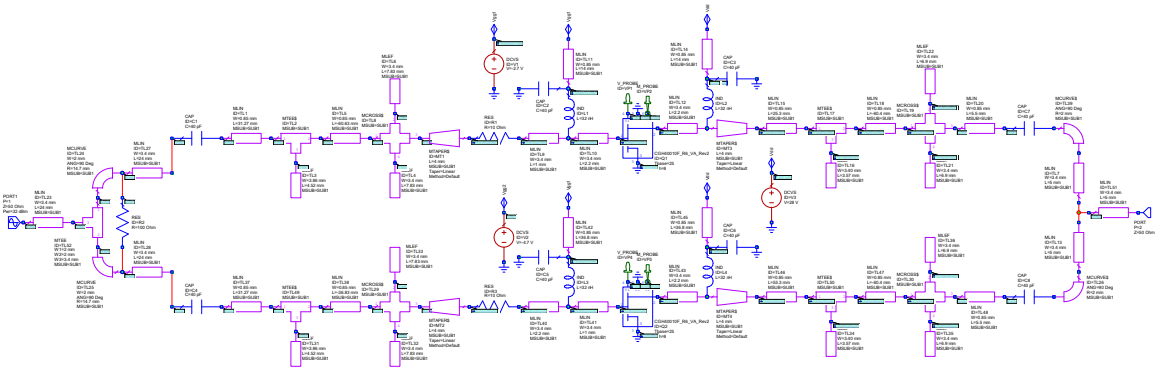


Fig. 5.11: Schematic of the proposed design.

Figure 5.11 illustrates the complete schematic of the proposed design.

The input and output return losses analyzed during the design with matching tool to make sure to achieve wide bandwidth. The tapered lines are utilized when there is width difference between two transmission lines to relax the bandwidth even more.

The reason that distributed elements are utilized is to make the fabrication process easier. Additionally, stub tuning is possible in post fabrication process with them. Moreover, using only open circuits was a constraint for the matching network rather than short-circuit stubs. This is to avoid the effects of additional vias. Moreover, if short-circuit stubs were

used, the post fabrication tuning would not be easy. Between the output of the power divider and the input matching circuit, surface mount capacitor is placed to block DC signal going into the transistor.

The output matching network is designed with the same method and constraints in mind. At the drain side of the transistor, a 2.2 mm long 50-ohm transmission line placed for a smooth connection for the transistor pin.

The rest of the network is realized with two open-stubs. The second open-stub that is closer to the output is divided equally to shorten the length as it was done in input matching circuit. Also, DC blocking capacitors are used in both end of the amplifiers. Then, the two amplifiers combined with 50-ohm lines to the output.

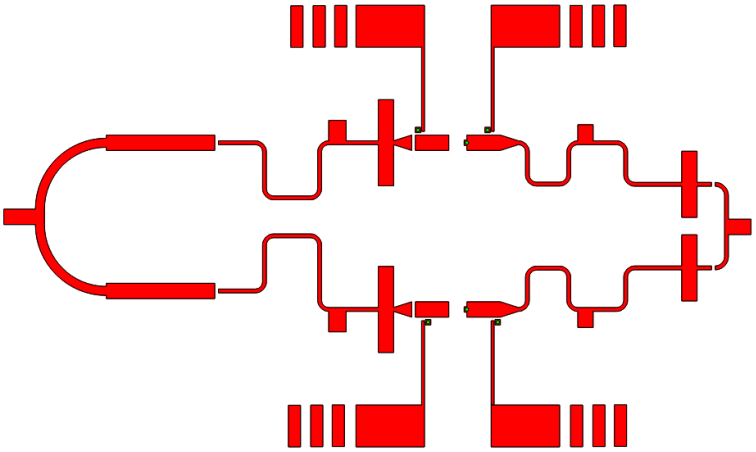


Fig. 5.12: Layout of the proposed design.

Figure 5.12 shows the layout of proposed design. At the input and output side of the both amplifiers, long transmission lines are meandered to save space. When meandering the lines, 90 degree sharp bends and chamfered are avoid to reduce the fabrication error. Instead curved bends with 90 degree angle are utilized.

Additionally, surface mount components pads adjusted to have reasonable spacing to solder properly and avoid any short circuit.

After layout process is finalized. The design is exported as a Gerber file to import into the milling machine via software. This circuit is fabricated using the LPKF ProtoMat S103

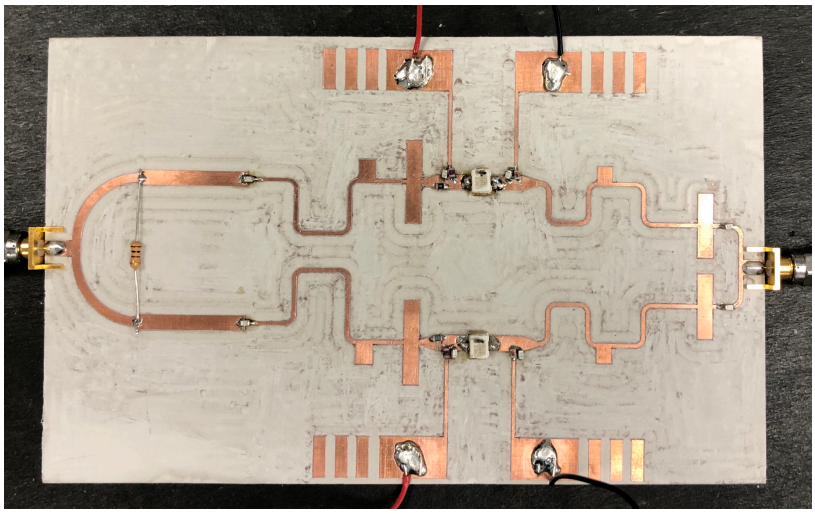


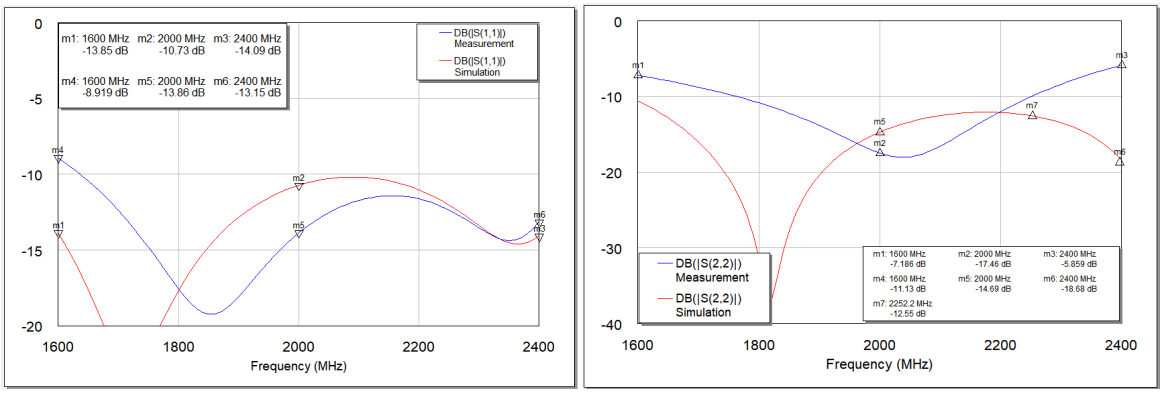
Fig. 5.13: Fabricated-modified Doherty-Like amplifier image.

milling machine at the CASE center at Syracuse University. Figure 5.13 presents the image of the fabricated circuit. The dimensions for the fabricated circuit is 160 x 100 mm or 1.06 λ x 0.66λ.

5.3 Experimental Results

The fabricated amplifier is tested between 1.6 - 2.4 GHz. Input power sweep applied to the design is between 26 - 34 dBm.

Figure 5.14 (a) show the comparison between simulated and measured input return loss.

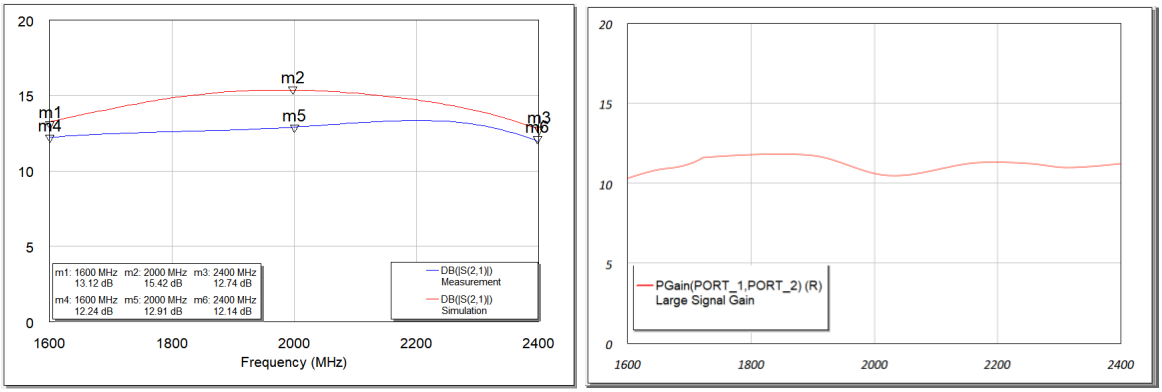


(a) Input return loss (b) Output return loss

Fig. 5.14: Simulation vs measurement of input and output return losses.

In the simulation, two center frequencies are appeared at 1.85 - 2.35 GHz and the overall performance is better than -10 dB. The measured result had a degradation on the performance and shift towards the center frequency. This might be due to parasitic effects of the active components in the matching networks. At the center frequency, input return loss is at -13.8 dB and the overall performance is better than -9 dB.

Figure 5.14 (b) presents the output return loss. It is showing similar behavior as in input return loss. At the center frequency, the design is achieving -17.46 dB and overall performance is better than -5.8 dB.Moreover, the design shows performance of better -10 dB between the frequency of 1.76 - 2.26 GHz.



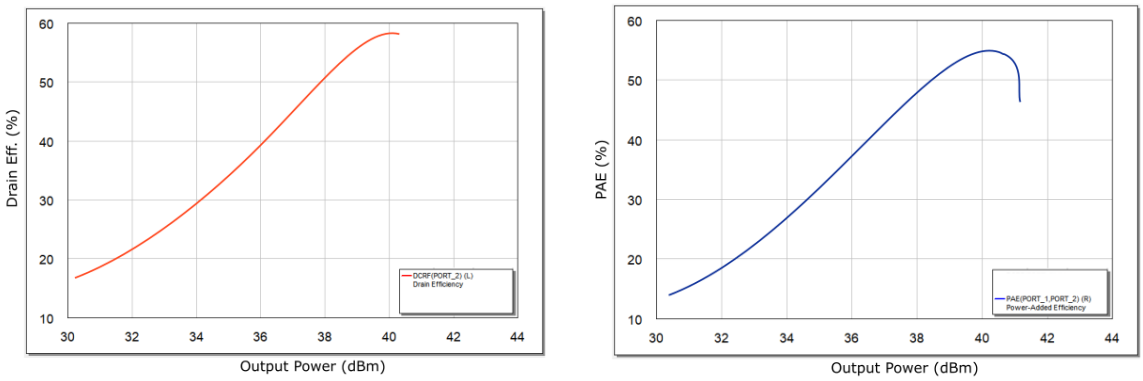
(a) Small-signal gain (b) Large-signal gain

Fig. 5.15: Small and large-signal gain results.

Figure 5.15 (a) illustrates the small signal gain comparison between simulation and measurement results. The small-signal gain is 12.9 dB at center frequency and the overall performance is better than 12.1 dB. Figure 5.15 (b) presents the measurement results of large-signal (power) gain respect to frequency. When the input power is at 32 dBm, the overall power gain is better 10 dB with a flat performance. Moreover, the design is providing the minimum power gain of 10.3 and the maximum value of 12.8 dB.

Figure 5.16 (a) shows the performance result of drain efficiency respect to output power. The design provides 58% drain efficiency at saturated power of 40.4 dBm.

Furthermore, Figure 5.16 (b) presents the result of power-added efficiency. At the center frequency, the maximum PAE has the value of 54% with the saturation power of 41.4 dBm.



(a) Drain efficiency (b) Power-added efficiency

Fig. 5.16: Drain and power added efficiency vs output power.

Table 5.3 provides performance comparison of broadband and high efficiency amplifier studies. These designs are using GaN transistors and operating at L- and S- frequency bands. The proposed design of this work provides improved bandwidth while achieving higher drain efficiency and saturated power level.

Table 5.3: Performance comparison of broadband and high efficiency amplifier studies

Refs.	**Year**	**Transistor**	**Freq. (GHz)**	**FBW (%)**	**PAE (%)**	**OBO Power (dB)**	**Psat (dBm)**	**Gain (dB)**
[93]	2012	10-W GaN	3-3.6	18	38	6	43	∼10
[95]	2012	10-W GaN	1.96-2.46	23	40	6	N/A	∼7
[98]	2014	10-W GaN	0.7-0.95	30	42	6	33.5	15
[101]	2015	15-W GaN	1.7-2.75	47	42.5	6	N/A	>8.5
[103]	2017	Gan	3-3.6	18	46	>7	N/A	12
This work	**2020**	**10-W GaN**	**1.6-2.4**	**40**	**39**	**6**	**41.4**	**10.3**

5.4 Conclusion

In this chapter, the design procedure and fabrication process for a Doherty-like amplifier, using a 10 W GaN transistor, is explained. The proposed amplifier is designed to achieve wider band width and higher efficiency over the operating frequency. The theory is based on the elimination of impedance inverter to achieve wide bandwidth. The analysis of the

transistor is completed to determined the optimum source and load impedances to design the input and output matching networks.

To validate the design approach, a 10-W modified Doherty-like amplifier is design, fabricated, and tested. The measurement results show that the proposed design is providing maximum PAE value of 54%, fractional bandwidth of 40%, and minimum power gain of 10.3 dB. Additionally, the proposed design is compared with other broadband DPA studies to see its performance.

CHAPTER 6
CONCLUSION AND FUTURE WORK

The conclusion of this study in a brief summary is presented in this chapter. Additionally, contributions and the future research ideas are discussed.

6.1 Conclusion

The exponential rise in the data usage and the number of wireless devices lead to use the frequency spectrum efficiently as it has been already over-utilized. Therefore, researchers and engineers focused on the design of better performing receivers and transmitters which are the main components of the wireless communication systems. In this study, the focus is to propose amplifier architectures to design broadband and high efficiency for LNA on the receiver side and PA on the transmitter side.

The theoretical overview and performance parameters about LNA and PA are introduced in Chapter 2. Moreover, Efficiency enhancement techniques for PA such as EER, ET, Outphasing, and Doherty as well as transistor technologies are discussed. in the same chapter.

Chapter 3 and chapter 4 are the proposed designs for LNA where as chapter 5 is designed for PA. The contributions of this study can be summarized as the following:

In chapter 3, a wideband low-noise amplifier operating at the center frequency of 2 GHz is designed, simulated, fabricated, and measured. The proposed design uses a high power gain BJT surface transistor. In order to achieve low noise figure, lumped elements avoided to use and microstrip technology is utilized as IMN and OMN are realized with only distributed elements. Reflection coefficients are calculated to obtain maximum transducer gain. Additionally, high and low impedance pads are used along with RF chokes as passive DC bias network for the selected transistor. Measured results show that the proposed design provides a wide bandwidth, low noise figure, moderate gain and sufficient input return loss in comparison to mentioned studies.

In chapter 4, a low VSWR wideband amplifier operating at the center frequency of 3 GHz is presented with simulation and measurement results. The design uses a unilateral, four-pin dual emitter BJT transistor. Same design methods used in the work as in chapter 3. Reflection coefficients for IMN and OMN are calculated and selected from the transistor's unconditionally stable region. R-L-C components are not utilized in the matching circuits as the parasitic effects of these components add to the noise figure. Eventually, with the careful fabricating process, simple architecture and steady performance is achieved.

In chapter 5, modified Doherty power amplifier architecture is proposed. The design is operating at the center frequency of 2 GHz and using 10 W GaN transistor. As stated previously, high efficiency and broadband amplifiers are needed in the transmitters to ensure high performance in the communication systems. In the conventional Doherty amplifier quarter wave impedance inverter is the main factor of the bandwidth limitation. In order to overcome this problem, the proposed design suggests that eliminating the quarter wave impedance to achieve broader bandwidth. After the elimination of the impedance inverter, the main and peak amplifier outputs are matched to optimum impedance to ensure smooth transition between the input and the output of the amplifier. Design of the IMN and OMN are based on the distributed elements including tapered lines. Moreover, in the input side, even split Wilkinson PD is designed.

Simulation and measurement results show that the proposed design provides 40% fractional bandwidth as it achieves maximum output power of 41.4 dBm, and 44% PAE at 6-dB back-off power level.

6.2 Future Work

The proposed architectures in this study can be extended. In chapter 3 and chapter 4, the proposed amplifiers are designed as a single stage. Possible future work might be to analyze multiple stages or cascodes in LNAs.

In addition to multi-stage design, discrete designs with different transistor technologies can be explored. Another possible future work area would be to analyze integrated circuit (IC) or monolithic ICs for LNAs for fifth generation, 5G, communication systems.

Furthermore, the designs utilize passive DC bias network that is based high and low impedance pads. Optimization about the location of these pads can be studied.

In chapter 5, the modified Doherty power amplifier is a symmetrical design. For a future work, asymmetric designs can be studied. Moreover, input power optimization and dual input drive can be analyzed to increase output power of the overall system.

The LNAs and PA in this study is designed to operate at L- and S- band. There are still research ideas to work on below 6 GHz frequency band. However, the new trend is going towards the higher frequencies with the 5G developments such as 28 GHz. There challenges about manufacturability. These challenges could be possible areas to work on.

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- Engineering Intern, TTM Technologies, Inc.