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Fault Coverage Measurement Technique for Analog Circuits

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REPORT

on

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30 March 1992

The purpose of this report is to fulfill the Master's Project requirement for the M.S. (Electrical Engineering) degree (plan B, engineering investigation).

Faculty Advisor: Prof. Jia
Approved: _____
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SUMMARY

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Measurement of a test sequence's fault coverage plays an important role in the specification of complex digital microcircuits. On the other hand, analog test engineers have not enjoyed the same benefit of being able to quantify how well a test sequence detects faults in an analog microcircuit. This fact of life is mainly due to the non-deterministic nature of analog signals. Other factors which have prohibited meaningful measurement of fault coverage in analog circuits include the effect of nominal component variations on circuit response and the widely-varied types of circuit functions that exist. In most cases the development of a thorough test set for even simple analog circuits is based on an ad-hoc collection of sometimes redundant tests. Test specifications are developed based on the circuit's function alone, without regard to the actual circuit architecture employed. With an increase in the complexity of analog circuits, and with the development of complex analog semicustom devices, it is becoming painfully apparent that there is a strong need to actually quantify fault coverage for analog circuits.

In an effort to define methods for performing fault simulation and measuring fault coverage in analog and mixed-mode circuits, techniques have been developed for defining a "fault dictionary" for a particular circuit, which accounts for the circuit's nominal component variations. This technique has been used by the author in an attempt to develop techniques for measuring the fault coverage that typical analog test methods provide for a particular analog device. A simplified operational amplifier test circuit model containing a transistor-level model of the device under test (DUT) is simulated and the output of the test circuit recorded in the fault dictionary. Faults are then singly inserted into the DUT and the data representing the unknown circuit condition is analyzed. Based on the fault dictionary, a statistically-based "guess" is made as to whether the circuit is faulted or not. Consistently incorrect results indicate a fault that the test circuit does not propagate to the test circuit output. This fault is referred to as one which is not "covered" by the test sequence, i.e. the test sequence does not have fault detection coverage for this fault. Expanding this methodology to an entire test sequence for an entire fault set will yield a measure of fault detection coverage.

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Abstract

This report describes an effort to develop a technique for measuring the amount of fault detection coverage that an analog test pattern has for a particular analog device. The technique is based on a software tool which statistically analyzes data from a circuit simulator. One example of a fault simulation experiment is presented, and some of the results are discussed. Finally, some ideas for future work in this area are given.

Contents

Introduction

Measurement of a test pattern's fault coverage plays an important role in the specification of complex digital microcircuits. Unfortunately, analog test engineers have not enjoyed the same benefit of being able to quantify how well a test pattern detects faults. This unfortunate fact can be attributed to the non-deterministic nature of analog signals and the inability to represent physical faults in a small number of fault classes (for example, stuck-at faults represent a large number of physical faults in digital logic circuits). Other factors which have prohibited meaningful measurement of fault coverage in analog circuits include the effect of nominal component variations on circuit response, the lack of mature analog simulators, and the wide variety of circuit functions that exist. In most cases, the development of a thorough test pattern for even simple analog circuits is based on an ad-hoc collection of sometimes redundant tests. Test specifications are developed based on the circuit's *function,* without regard to the circuit's *architecture.* Increases in the complexity of analog microcircuits and the advent of analog application-specific integrated circuits (ASIC), are pointing to the need for being able to quantify test quality and develop test patterns which account for circuit topology.

Background

Fault analysis of analog circuits has been an active research area for many years. Literature surveys[1] show that the Department of Defense (DoD) has held a small but steady interest in this area since the beginning of the 1960s. Early efforts were designed to ease the task of isolating component failures on circuit cards containing analog circuitry. Later efforts had goals ranging from fault-driven automatic test pattern generation (ATPG) to built-in self test (BIST). The author's involvement in this area has been with more general goals in mind. First, to develop an understanding of the basic problems associated with the simulation of faults in analog circuits, and second, to investigate various methods of fault analysis. In May 1989, the U. S. Air Force's Rome Laboratory (RL) awarded an eighteen-month contract to David Sarnoff Research Center (DSRC) to research the state-of-the-art and develop a specific technique of analyzing analog circuit faults. The result is the methodology embodied by the Statistical Fault Analyzer (SFA).[2,3]

SFA Basics

The SFA is a software tool which provides data analysis and circuit faulting capabilities to a circuit simulator such as SPICE 3C1. It consists of a preprocessor which directs the simulation according to a set of control statements included in the simulator input file. These control statements describe how the circuit is to be faulted, the number of simulations to be run, and what information will form the output file. Gaussian component variations are specified by allowing any numerical value in the SPICE input (except node numbers) to be replaced by a mean and standard deviation value. The SFA also contains a post-processor to collect and format the output from the simulation. The SFA can post-process any numerical result of the simulation including nodal voltages, branch currents, frequency response, and transient data. The resulting files may be analyzed using two different statistical methods: hypothesis testing for fault detection and discrimination analysis for fault classification. For the purposes of this discussion, only hypothesis testing (fault detection) will be discussed.

Hypothesis Testing

For hypothesis testing, the SFA generates a data file containing simulation results for an unfaulted circuit. It usually contains many entries, each one slightly different due to component variations introduced through Monte Carlo methods. The data file is a multivariate distribution representing the circuit's unfaulted behavior. This distribution forms the basis for the null hypothesis, H_o, which states that the circuit is good or unfaulted. When simulation results from a faulted circuit are presented to the SFA, a hypothesis test is used to calculate the probability that the faulted response lies within the unfaulted distribution. If this probability is less than a predetermined threshold (confidence level), H_o is rejected and the fault is detected. Otherwise, H_o is incorrectly accepted, indicating that the fault may be undetectable. Incorrect acceptance of H_o is known as a Type II error and may be due to a truly undetectable fault or an ill-defined unfaulted distribution. Consistent rejection of H_o, allowing for the expected number of Type II errors, indicates that the faulted circuit's response is distinguishable from the unfaulted circuit's response. When this is the case, the fault is detectable and the test that achieved the detection is said to "cover" the fault.[4]

Fault Detection Coverage

Fault detection coverage is a measure of a test method's ability to detect faults in the device under test (DUT). For analog circuits, a test method defines the forcing functions applied to the DUT and specifies the external test circuitry used. Analog fault detection coverage is dependent on the test pattern, the faults selected, and the test circuit. Thus, any measure of fault detection coverage for analog circuits must specify the entire test method, as well as the fault set used. Fault detection coverage is reported as a ratio of the number of detected faults to the total number of faults possible in the DUT. In the most general sense, the total number of faults possible would include combinations of individual faults, resulting in an astronomical number of circuit states. For simplicity, this investigation considers only "one-at-a-time," or singly-inserted faults.

Experiment Description

For this study, the hypothesis test routine contained in the SFA is used to determine if it is possible to measure the amount of fault detection coverage that specific analog test methods have for a given analog circuit. Before the actual experiment and results can be discussed, elements of the setup must be described. The elements used for this experiment include the DUT, the test circuit, and the fault set.

DUT Description

The DUT used in this experiment is a commercially available macrocell operational amplifier (MOPA). This macrocell is a part of the Raytheon Linear Array (RLA) series of analog ASICs. The selection of this device as a test case is based on two main factors. First, analog ASICs present an acute challenge with respect to developing quality tests. With standard single analog functions, it may be acceptable to have a function-driven, general-purpose test pattern that contains testing redundancies. However, when these functions are combined into large specialized circuits, as is the case with many analog ASICs, it is no longer acceptable to have an inefficient test pattern. Components of the test pattern must provide the most "bang for the buck" and be as independent as possible regarding the information

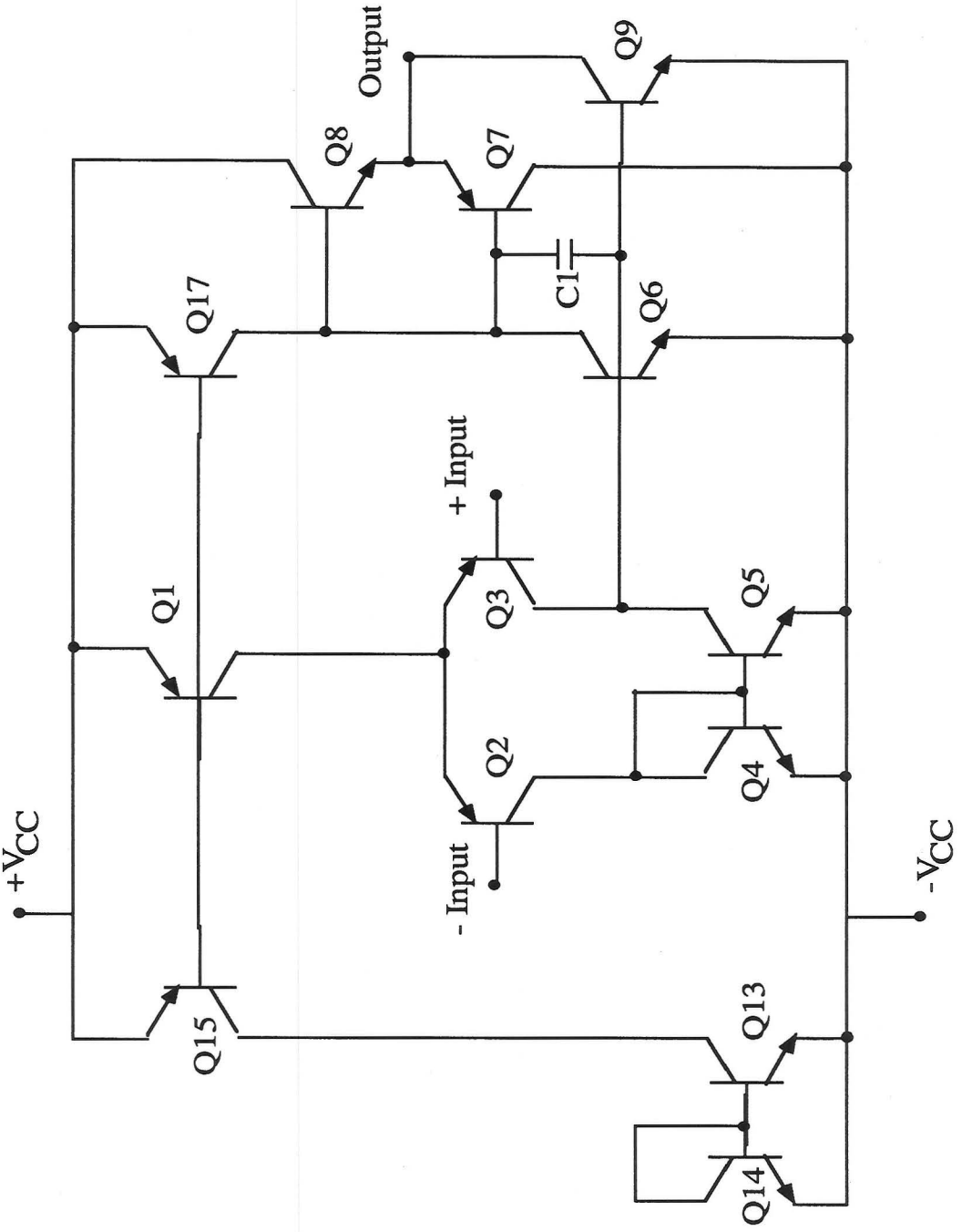

Figure 1. D.U.T. Transistor-level Circuit.[6]

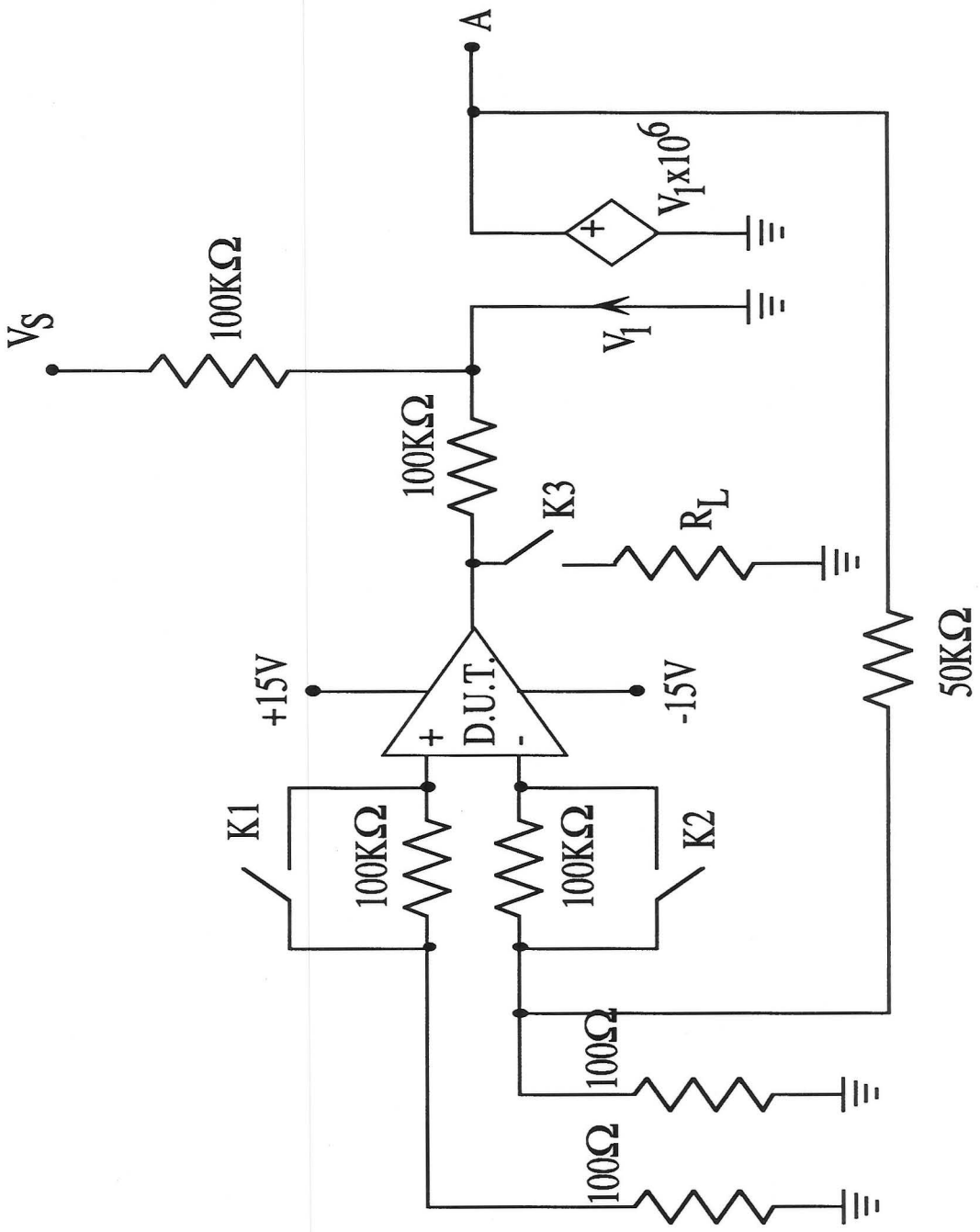

Figure 2. Test Circuit Containing D.U.T.

provided about the state of the circuit. At the same time, they must together give a complete and accurate evaluation of the DUT. In choosing the MOPA as the test case, it was recognized that in order to assess test quality for combinations of these functions, one must first master assessment of individual functions. The second reason for selecting this particular family of circuits is that they have a strong relevance to analog military microelectronics. The RLA family of devices is the first analog semi-custom parts to achieve qualification under the Joint Army-Navy (JAN) MIL-M-38510 specification system for microcircuits.[5] This specification opens the door for widespread use of these devices in military systems. For this reason, it is in our best interest to seek better means of evaluating test quality for these devices. Figure 1 shows the MOPA internal architecture.

Test Circuit Description

In analog testing, the test circuit plays an extremely vital role in determining if faulty DUT behaviors are propagated to the measurement points. In fact, the test circuit is every bit as important to fault coverage as the test pattern is. For this reason, the test circuit must be grouped along with the DUT for any fault simulations. The test circuit selected for this investigation is a simplified operational amplifier test loop, such as those found on MIL-M-38510 analog detail specifications and in MIL-STD-883 analog test methods. The main point that distinguishes the DUT and the test circuit during simulation is that the DUT must be modeled structurally so that component faults can be inserted, whereas the test circuit may be modeled behaviorally or as a macro model since it is assumed that the test circuit contains no faults. Additionally, we assume that the test circuit is fixed and cannot be altered as a way of increasing fault coverage. However, note that alteration of the test circuit may very well be an excellent method of increasing fault coverage. A schematic of the test circuit containing the DUT appears in figure 2.

The schematic of figure 2 shows the DUT in a standard operational amplifier test circuit. Input patterns to this test circuit consist of applying a forcing voltage at V_s and opening or closing relays K1, K2, or K3. The output is measured at test point A. The tests that were implemented and their associated test patterns are shown in Table 1. Due to computational limitations, a full operational amplifier test suite was not applied, but will be in future investigations.

Test	Test Pattern (V_S,K1,K2,K3)	Measure Point (fig. 2)
V_{OS}	0V, closed, closed, open	A
I_{OS}	0V, open, open, open	A
$+I_{IB}$	0V, closed, open, open	A
$-I_{IB}$	0V, open, closed, open	A
A_V	0V, closed, closed, closed	A

Table 1. Test Pattern Description.

Fault Set Selection

Selection of a realistic fault set for analog circuits (and perhaps for high-speed digital circuits) is a very difficult process. Very limited data is available on the types of faults which commonly occur in these circuits. For example, an Air Force study[7] reports that 32% of IC failures are due to opens, 22% are due to shorts, and 18% are due to parametric or "soft" faults such as low gain. However, no breakdown is given for the type of structure or type of device (analog or digital) that the faults occurred in. Also, this data comes from field failures and may not be comparable to manufacturing defect data. In an attempt to remedy this situation, an effort[8] is underway which is exploring the possibility of utilizing microcircuit defect simulators to generate a list of manufacturing faults prioritized by probability of occurrence. At the present time however, this approach is not well-defined and in this experiment the fault set selection was based solely on reasonable engineering judgement. For each transistor of the DUT, seven faults are considered. Each transistor lead (base, emitter, collector) can be shorted to each of the two remaining leads (3 faults), each lead can have a high resistance (3 faults), or the transistor's forward current gain ($ß_F$) can be low (1 fault). This makes a total of 91 faults possible throughout the circuit. Note that this fault set is not intended to represent the actual faults that can occur in this device. It is used only for proof-of-concept purposes until a more realistic fault set can be developed.

Simulation

Once the DUT, test circuit, and fault set have been defined and coded into the SFA input format, fault simulations may be run. For fault detection coverage analysis, which uses the basic hypothesis test, the circuit's nominal behavior must be defined. In this case, the unfaulted circuit is simulated a total of 100 times while introducing a 10% normal variation into each transistor's forward current gain ($ß_F$) and Early voltage (V_A). Previous sensitivity analyses[1] show that these two parameters have the most significant effect on transistor performance. The circuit is then simulated 100 times for each single fault condition. A hypothesis test is performed after each simulation. This procedure is iterated for each test condition considered. Results of the fault simulation indicate how many times H_o was accepted or rejected for each fault and test condition.

Initial Results

Results to date have shown many examples of faults that are detected by one test pattern, and not another. For example, simulations (see appendix A for listings and summarized outputs) show that the offset voltage test (V_{OS}) cannot distinguish between the nominal circuit and the circuit with a short inserted between the collector and base or collector and emitter of transistor Q5 (see figure 1). This is apparent from fault simulations where the V_{OS} test correctly accepts H_o 94% of the time when the circuit is nominal, yet incorrectly accepts H_o 92-95% of the time when the faults are present. On the other hand, the offset current (I_{OS}) test is able to detect these faults by causing the fault to propagate to the circuit output. I_{OS} also correctly accepts H_o during unfaulted runs, but rejects H_o 100% of the time when the faults are inserted. One can conclude from this that the I_{OS} test has fault detection coverage for these faults, while the V_{OS} test does not. Expanding this methodology to an entire test sequence for an entire fault set yields a measure of fault detection coverage or test quality.

Future Investigations

There are several areas which offer opportunities for additional investigation. First, focusing on refining the SFA methodology and researching practical methods of defining a fault set for a given circuit will increase the practicality of the SFA. Second, continued work on using the SFA tool to define techniques for measuring fault coverage, such as simulation of a full operational amplifier test suite will further reinforce the concept of analog fault coverage. Also, better means of generating practical analog fault sets would make the SFA much more useful. Eventually, it is hoped that these measurement techniques will be standardized in the same way that digital techniques have been in MIL-STD-883, Procedure 5012: "Fault Coverage Measurement for Digital Microcircuits."[9]

Conclusions

Initial results from an analog fault simulation experiment show that it is possible to measure the amount of fault detection coverage that a specific test method has for a given analog circuit. The method requires a transistor-level model of the DUT, a model of the test circuit, and a fault set in terms of component value or model parameter value modifications. Fault detection coverage is measured by taking the ratio of the number of faults detected by the hypothesis test to the total number of faults in the fault set. Additional work is needed in defining a realistic fault set and in extending the method to a complex analog ASIC containing many function modules.

References

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2. B. R. Epstein, M. H. Czigler, and S. R. Miller, "Linear Microcircuit Fault Modeling and Simulation (Final Report)," *RL-TR-91-106,* Rome Laboratory, Griffiss AFB NY, June 1991.
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4. B. W. Johnson, *Design and Analysis of Fault-Tolerant Digital Systems,* Reading, MA, Addison-Wesley, 1989.
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8. E. P. Ratazzi, "Statement of Work for Analog Microcircuit Fault Prediction," in *Purchase Request N-2-5723,* Rome Laboratory, Griffiss AFB NY, September 1991.
9. W. H. Debany, K. A. Kwiat, H. B. Dussault, M. J. Gorniak, A. R. Macera, and D. E. Daskiewich, "Fault Coverage Measurement for Digital Microcircuits," *Test Procedure 5012 of MIL-STD-883 (Notice 12),* Rome Laboratory, Griffiss AFB NY, 27 July 1990.

Appendix A

This appendix contains an SFA input file listing and two summary statistics output listings from the SFA.

Listing 1 shows the SFA input file used for this experiment. Comments are included to describe some of the SFA-specific syntax used. For a full description of the SFA control statements, see reference [2]. For a complete description of the SPICE 3C1 syntax, see the SPICE 3 users guide.

Listing 2 contains the summary output from the SFA run corresponding to the V_{os} test. Note that the hypothesis test statistics indicate excellent results for the NOMINAL case, while very poor results are achieved for the Q5CBS (short between Q5's collector and base) case. This indicates that the V_{os} does not posses fault detection coverage for this fault. Note that classification results are poor also.

Listing 3 is the summary output for the I_{os} test. Note that these hypothesis test results are very good for both the NOMINAL case as well as the fault Q5CBS. This indicates that the I_{os} test has fault detection coverage for this fault. It is also interesting to note that this test was able to correctly classify the fault 100% of the time. However, one should be cautious not to conclude from the good classification result that I_{os} has fault *location* coverage for Q5CBS. When other faults are considered, the detection (hypothesis test) results may remain high, but misclassification *between faults* would most likely increase.

```
OP AMP TEST LOOP FOR DC PARAMETER MEASUREMENT OF MOPA1
*
*START OF FAULT ANALYZER CONTROL SECTION.  THE
*FOLLOWING COMMENTS DESCRIBE THE DIFFERENT TYPE
*OF SFA CONTROL STATEMENTS THAT ARE USED.
*
*   #GOOD <number_of_runs>
*      DIRECTS THE SFA TO SIMULATE THE CIRCUIT
*      WITH NO FAULTS FOR THE NUMBER OF TIMES
*      SPECIFIED.  NOMINAL COMPONENT VARIATIONS
*      ARE INTRODUCED USING MONTE CARLO
*      TECHNIQUES.
*
*   #<component_name> <faulted_value> <number_of_runs>
*                                  <fault_name>
[<model_parameter>]
*      DIRECTS THE SFA TO FAULT THE COMPONENT
*      NAMED BY REPLACING THE UNFAULTED VALUE
*      WITH THE GIVEN FAULTED VALUE.  THE RESULTING
*      FAULTY CIRCUIT IS SIMULATED FOR THE NUMBER
*      OF TIMES SPECIFIED.  NOMINAL COMPONENT
*      VARIATIONS ARE INTRODUCED INTO OTHER
*      UNFAULTED COMPONENTS.  IF THE FAULTED VALUE
*      CORRESPONDS TO A MODEL PARAMETER WITHIN
*      A DEVICE MODEL, THE NAME OF THE MODEL
*      PARAMETER SHOULD BE GIVEN.
*
*   %dc <node_value> [<node_value> <node_value> ...]
*      CAUSES THE SFA TO USE THE DC NODE VALUES
*      SPECIFIED FOR FAULT ANALYSIS.  MUST SPECIFY
*      .OP IN INPUT FILE.
*
*   %ac <node_value> [<node_value> <node_value> ...]
*      CAUSES THE SFA TO USE VECTORS FROM AN
*      AC ANALYSIS FOR FAULT ANALYSIS.  MUST
*      SPECIFY .AC IN INPUT FILE.
*
*   %polar
*      CAUSES THE SFA TO STORE RESULTS IN POLAR
*      NOTATION.  THE DEFAULT IS RECTANGULAR FORM.
*
```

Listing 1. SFA Input File (continued).

```
*   ANY NUMERICAL VALUE EXCEPT NODE NUMBERS MAY BE
*   GIVEN A STATISTICAL VALUE BY REPLACING THE
*   VALUE WITH [<mean>,<standard_deviation>].  THE ACTUAL
*   VALUE USED DURING SIMULATION WILL THEN BE
*   CALCULATED USING MONTE CARLO METHODS FOR EACH
*   GOOD AND FAULTED SIMULATION.
*
#GOOD 100
*
#RQ1CB 1.0 100 Q1CBS
#RQ1CE 1.0 100 Q1CES
#RQ1BE 1.0 100 Q1BES
#QPNPS1 1.0E8 100 Q1CO RC
#QPNPS1 1.0E8 100 Q1BO RB
#QPNPS1 1.0E8 100 Q1EO RE
#QPNPS1 1.0 100 Q1LOWB BF
*
#RQ2CB 1.0 100 Q2CBS
#RQ2CE 1.0 100 Q2CES
#RQ2BE 1.0 100 Q2BES
#QPNPS2 1.0E8 100 Q2CO RC
#QPNPS2 1.0E8 100 Q2BO RB
#QPNPS2 1.0E8 100 Q2EO RE
#QPNPS2 1.0 100 Q2LOWB BF
*
#RQ3CB 1.0 100 Q3CBS
#RQ3CE 1.0 100 Q3CES
#RQ3BE 1.0 100 Q3BES
#QPNPS3 1.0E8 100 Q3CO RC
#QPNPS3 1.0E8 100 Q3BO RB
#QPNPS3 1.0E8 100 Q3EO RE
#QPNPS3 1.0 100 Q3LOWB BF
*
#RQ4CB 1.0 100 Q4CBS
#RQ4CE 1.0 100 Q4CES
#RQ4BE 1.0 100 Q4BES
#QNPNS4 1.0E8 100 Q4CO RC
#QNPNS4 1.0E8 100 Q4BO RB
#QNPNS4 1.0E8 100 Q4EO RE
#QNPNS4 1.0 100 Q4LOWB BF
```

Listing 1. SFA Input File (continued).

```
#RQ5CB 1.0 100 Q5CBS
#RQ5CE 1.0 100 Q5CES
#RQ5BE 1.0 100 Q5BES
#QNPNS5 1.0E8 100 Q5CO RC
#QNPNS5 1.0E8 100 Q5BO RB
#QNPNS5 1.0E8 100 Q5EO RE
#QNPNS5 1.0 100 Q5LOWB BF
*
#RQ6CB 1.0 100 Q6CBS
#RQ6CE 1.0 100 Q6CES
#RQ6BE 1.0 100 Q6BES
#QNPNS6 1.0E8 100 Q6CO RC
#QNPNS6 1.0E8 100 Q6BO RB
#QNPNS6 1.0E8 100 Q6EO RE
#QNPNS6 1.0 100 Q6LOWB BF
*
#RQ7CB 1.0 100 Q7CBS
#RQ7CE 1.0 100 Q7CES
#RQ7BE 1.0 100 Q7BES
#QMPIS7 1.0E8 100 Q7CO RC
#QMPIS7 1.0E8 100 Q7BO RB
#QMPIS7 1.0E8 100 Q7EO RE
#QMPIS7 1.0 100 Q7LOWB BF
*
#RQ8CB 1.0 100 Q8CBS
#RQ8CE 1.0 100 Q8CES
#RQ8BE 1.0 100 Q8BES
#QNPNS8 1.0E8 100 Q8CO RC
#QNPNS8 1.0E8 100 Q8BO RB
#QNPNS8 1.0E8 100 Q8EO RE
#QNPNS8 1.0 100 Q8LOWB BF
*
#RQ9CB 1.0 100 Q9CBS
#RQ9CE 1.0 100 Q9CES
#RQ9BE 1.0 100 Q9BES
#QNPNS9 1.0E8 100 Q9CO RC
#QNPNS9 1.0E8 100 Q9BO RB
#QNPNS9 1.0E8 100 Q9EO RE
#QNPNS9 1.0 100 Q9LOWB BF
*
#RQ13CB 1.0 100 Q13CBS
```

Listing 1. SFA Input File (continued).


```
#RQ13CE 1.0 100 Q13CES
#RQ13BE 1.0 100 Q13BES
#QNPNS13 1.0E8 100 Q13CO RC
#QNPNS13 1.0E8 100 Q13BO RB
#QNPNS13 1.0E8 100 Q13EO RE
#QNPNS13 1.0 100 Q13LOWB BF
*
#RQ14CB 1.0 100 Q14CBS
#RQ14CE 1.0 100 Q14CES
#RQ14BE 1.0 100 Q14BES
#QNPNS14 1.0E8 100 Q14CO RC
#QNPNS14 1.0E8 100 Q14BO RB
#QNPNS14 1.0E8 100 Q14EO RE
#QNPNS14 1.0 100 Q14LOWB BF
*
#RQ15CB 1.0 100 Q15CBS
#RQ15CE 1.0 100 Q15CES
#RQ15BE 1.0 100 Q15BES
#QPNPS15 1.0E8 100 Q15CO RC
#QPNPS15 1.0E8 100 Q15BO RB
#QPNPS15 1.0E8 100 Q15EO RE
#QPNPS15 1.0 100 Q15LOWB BF
*
#RQ17CB 1.0 100 Q17CBS
#RQ17CE 1.0 100 Q17CES
#RQ17BE 1.0 100 Q17BES
#QPNPS17 1.0E8 100 Q17CO RC
#QPNPS17 1.0E8 100 Q17BO RB
#QPNPS17 1.0E8 100 Q17EO RE
#QPNPS17 1.0 100 Q17LOWB BF
*
#RC1S 1.0 100 C1S
*
*NODE 9 CORRESPONDS TO THE TEST LOOP OUTPUT POINT.
*SEE FIGURE 2, TEST POINT A.
%dc 9
*
*END OF SFA CONTROL SECTION.
*
*START OF TEST CIRCUIT.
*
```

Listing 1. SFA Input File (continued).

```
*OPERATING POINT ANALYSIS GIVES US DC VALUES AT ALL
*NODES.
.OP
*
*SUPPLY VOLTAGES (VSP, VSN) AND BIAS CURRENT (ISET).
VSP 10 0 DC +15V
VSN 11 0 DC -15V
ISET 10 5 +10UA
*
*LOOP CONTROL VOLTAGE (VS).  SEE TABLE 1 FOR VS
*SETTINGS.
VS 8 0 0V
*
*ENULL IS THE NULLING AMPLIFIER.  IT IS MODELED HERE
*AS AN SEMI-IDEAL AMPLIFIER WITH OPEN LOOP GAIN OF
*1,800,000.
ENULL 9 0 7 0 -1.8E6
*
*XDUT IS THE SUBCIRCUIT CALL TO OUR DEVICE UNDER
*TEST.
XDUT 4 3 11 6 10 5 MOPA1TX
*
*FOR K1 OPEN, SET RS2=100 KOHMS.  FOR K1 CLOSED, SET
*RS2=0.01 OHMS.  FOR K2 OPEN SET RS1=100 KOHMS.  FOR
*K2 CLOSED, SET RS1=0.01 OHMS.  SEE FIGURE 2 AND
*TABLE 1 FOR K1 AND K2 SETTINGS.
RS1 1 3 0.01
RS2 2 4 0.01
*
*R1, R2, R3, R4, C1, AND RF ARE FIXED-VALUE COMPONENTS
*OF THE TEST CIRCUIT.
R1 1 0 100
R2 2 0 100
R3 6 7 100K
R4 8 7 100K
C1 9 7 0.1UF
RF 9 2 49.9K
*
*LOAD RESISTOR (RL).  FOR K3 OPEN, COMMENT OUT RL.  FOR
*K3 CLOSED, LEAVE RL IN.  SEE FIGURE 2 AND TABLE 1 FOR
*K3 SETTINGS.
```

Listing 1. SFA Input File (continued).

```
*RL 6 0 10K
*
*START OF DUT SUBCIRCUIT.
.SUBCKT MOPA1TX      1   2   3   4   5   6
*                   (+) (-) -VS  VO +VS ISET
Q1 9 7 5 3 QPNPS1 0.2X
      RQ1CB 9 7 [1.0E8,0.0]
      RQ1CE 9 5 [1.0E8,0.0]
      RQ1BE 7 5 [1.0E8,0.0]
Q2 11 2 9 3 QPNPS2
      RQ2CB 11 2 [1.0E8,0.0]
      RQ2CE 11 9 [1.0E8,0.0]
      RQ2BE 2 9 [1.0E8,0.0]
Q3 12 1 9 3 QPNPS3
      RQ3CB 12 1 [1.0E8,0.0]
      RQ3CE 12 9 [1.0E8,0.0]
      RQ3BE 1 9 [1.0E8,0.0]
Q4 11 11 3 3 QNPNS4
      RQ4CB 11 11 [1.0E8,0.0]
      RQ4CE 11 3 [1.0E8,0.0]
      RQ4BE 11 3 [1.0E8,0.0]
Q5 12 11 3 3 QNPNS5
      RQ5CB 12 11 [1.0E8,0.0]
      RQ5CE 12 3 [1.0E8,0.0]
      RQ5BE 11 3 [1.0E8,0.0]
Q6 13 12 3 3 QNPNS6
      RQ6CB 13 12 [1.0E8,0.0]
      RQ6CE 13 12 [1.0E8,0.0]
      RQ6BE 12 3 [1.0E8,0.0]
Q7 3 13 4 3 QMPIS7
      RQ7CB 3 13 [1.0E8,0.0]
      RQ7CE 3 4 [1.0E8,0.0]
      RQ7BE 13 4 [1.0E8,0.0]
Q8 5 13 4 3 QNPNS8
      RQ8CB 5 13 [1.0E8,0.0]
      RQ8CE 5 4 [1.0E8,0.0]
      RQ8BE 13 4 [1.0E8,0.0]
Q9 4 12 3 3 QNPNS9
      RQ9CB 4 12 [1.0E8,0.0]
      RQ9CE 4 3 [1.0E8,0.0]
      RQ9BE 12 3 [1.0E8,0.0]
```

Listing 1. SFA Input File (continued).

```
+ XTB=1.7 NE=1.4 BR=19 VAR=9.0 IKR=3.57E-4 ISC=1.0E-16 NC=1.2
RB=[161.0,0.0]
+ RE=[1.9,0.0] RC=[235.0,0.0] CJE=5.52E-13 VJE=0.75 MJE=0.34
CJC=2.89E-13 VJC=0.6
+ MJC=0.42 CJS=1.39E-12 VJS=0.47 MJS=0.32 XCJC=0.5 TF=2.0E-10
TR=5.0E-9)
*
.MODEL QNPNS14 NPN (IS=5.2E-16 BF=[250.0,25.0] VAF=[130.0,13.0]
IKF=1.44E-2 ISE=1.61E-16
+ XTB=1.7 NE=1.4 BR=19 VAR=9.0 IKR=3.57E-4 ISC=1.0E-16 NC=1.2
RB=[161.0,0.0]
+ RE=[1.9,0.0] RC=[235.0,0.0] CJE=5.52E-13 VJE=0.75 MJE=0.34
CJC=2.89E-13 VJC=0.6
+ MJC=0.42 CJS=1.39E-12 VJS=0.47 MJS=0.32 XCJC=0.5 TF=2.0E-10
TR=5.0E-9)
*
.MODEL QPNPS1 PNP (IS=6.3E-16 BF=[155.0,15.5] VAF=[60.0,6.0]
IKF=1.0E-4 ISE=1.25E-15
+ XTB=0.55 NE=1.5 BR=27 VAR=18.6 IKR=3.0E-5 ISC=4.74E-16 NC=1.2
RB=[540.0,0.0]
+ RE=[45.0,0.0] RC=[575.0,0.0] CJE=1.7E-13 VJE=0.41 MJE=0.16
CJC=6.8E-13 VJC=0.54
+ MJC=0.37 TF=3.5E-8 PTF=20 TR=7.0E-7)
*
.MODEL QPNPS15 PNP (IS=6.3E-16 BF=[155.0,15.5] VAF=[60.0,6.0]
IKF=1.0E-4 ISE=1.25E-15
+ XTB=0.55 NE=1.5 BR=27 VAR=18.6 IKR=3.0E-5 ISC=4.74E-16 NC=1.2
RB=[540.0,0.0]
+ RE=[45.0,0.0] RC=[575.0,0.0] CJE=1.7E-13 VJE=0.41 MJE=0.16
CJC=6.8E-13 VJC=0.54
+ MJC=0.37 TF=3.5E-8 PTF=20 TR=7.0E-7)
*
.MODEL QPNPS17 PNP (IS=6.3E-16 BF=[155.0,15.5] VAF=[60.0,6.0]
IKF=1.0E-4 ISE=1.25E-15
+ XTB=0.55 NE=1.5 BR=27 VAR=18.6 IKR=3.0E-5 ISC=4.74E-16 NC=1.2
RB=[540.0,0.0]
+ RE=[45.0,0.0] RC=[575.0,0.0] CJE=1.7E-13 VJE=0.41 MJE=0.16
CJC=6.8E-13 VJC=0.54
+ MJC=0.37 TF=3.5E-8 PTF=20 TR=7.0E-7)
*
```


Listing 1. SFA Input File (continued).

```
.MODEL QMPIS7 PNP (IS=1.38E-15 BF=[250.0,25.0] VAF=[100.0,10.0]
IKF=2.56E-4 ISE=4.08E-15
+ XTB=0.55 NE=1.7 BR=0.22 VAR=19 IKR=1.82E-6 ISC=5.21E-14
RB=[100.0,0.0]
+ RE=[50.0,0.0] RC=[122.0,0.0] CJE=1.79E-13 VJE=0.41 MJE=0.22
CJC=2.39E-12
+ VJC=0.48 MJC=0.32 TF=1.0E-8 TR=9.5E-8 NC=1.14)
*
.ENDS MOPA1TX
*END OF DUT SUBCIRCUIT
*
.END
*END OF TEST CIRCUIT
```

Listing 1. SFA Input File (continued).

```
SUMMARY STATISTICS FOR GROUP NOMINAL:
  Classification success out of 100 runs:
     class NOMINAL: 73 ( 73.0 %)
     class Q5CBS: 27 ( 27.0 %)

  Hypothesis test success rate: 94 out of 100 (or  94.0 %)


SUMMARY STATISTICS FOR GROUP Q5CBS:
  Classification success out of 100 runs:
     class NOMINAL: 69 ( 69.0 %)
     class Q5CBS: 31 ( 31.0 %)

  Hypothesis test success rate: 5 out of 100 (or   5.0 %)


CUMULATIVE STATISTICS:
    Total correct classification was 104 out of 200 (or  52.0 %)
    Total # of correct hyp. tests was 99 out of 200 (or  49.5 %)
    Null hypothesis assumes test data is NOMINAL
    Type I errors = false rejection of null hypothesis = 6
    Type II errors = false acceptance of null hypothesis = 187
    Starting random number seed = -1
    Vector elements used:
     1
```

Listing 2. Summary Output for V_{os} Test.

```
SUMMARY STATISTICS FOR GROUP NOMINAL:
  Classification success out of 100 runs:
     class NOMINAL: 100 (100.0 %)
     class Q5CBS: 0 (  0.0 %)

  Hypothesis test success rate: 95 out of 100 (or  95.0 %)


SUMMARY STATISTICS FOR GROUP Q5CBS:
  Classification success out of 100 runs:
     class NOMINAL: 0 (  0.0 %)
     class Q5CBS: 100 (100.0 %)

  Hypothesis test success rate: 100 out of 100 (or 100.0 %)


CUMULATIVE STATISTICS:
    Total correct classification was 200 out of 200 (or 100.0 %)
    Total # of correct hyp. tests was 195 out of 200 (or  97.5 %)
    Null hypothesis assumes test data is NOMINAL
    Type I errors = false rejection of null hypothesis = 5
    Type II errors = false acceptance of null hypothesis = 0
    Starting random number seed = -1
    Vector elements used:
     1
```

Listing 3. Summary Output for I_{os} Test.