2011

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Recommended Citation

P. Feng and P. Ghosh, "Comparison of silicon-on-insulator and Body-on-Insulator FinFET based digital circuits with consideration on self-heating effects," in 2011 International Semiconductor Device Research Symposium, ISDRS 2011, December 7, 2011 - December 9, 2011, College Park, MD, United states, 2011.

Student Paper

Comparison of Silicon-on-Insulator and Body-on-Insulator FinFET Based Digital Circuits with Consideration on Self-Heating Effects

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In recent years FinFET emerges as a promising device to assure the desired performance in the sub-22 nm regime. Among various FinFETs, SOI FinFET shows suppressed leakage current and superior short channel effects. However, it suffers from increased self-heating effect (SHE) due to the adaptation of a low thermal conductivity buried silicon dioxide layer and a ultra thin fin body. Bulk FinFET, on the other hand, mitigates the heating issue at the cost of the leakage current. Body-on-Insulator (BOI) FinFET alleviates, to some extent, the aforementioned downsides of both SOI and bulk FinFET but with the increased fabrication complexity [1]. Here, we report extensive simulation of BOI and SOI FinFETs using technology computer aided design (TCAD) [2] and for the first time, present evaluation of BOI and SOI FinFET based digital circuits and demonstrate that in actuality SHE is comparable for both circuits under low voltage bias.

Both 3-D BOI and SOI FinFETs are designed with 25 nm gate length, 0.7 nm equivalent oxide thickness, 15 nm fin width and 50 nm fin height as shown in Fig. 1 [3]. The channel is lightly doped at 10^{15} cm-3 and the S/D region at 10^{19} cm-3. Philips unified mobility model, quantization model and hydrodynamic transport model are included to consider quantum effects, temperature dependence of mobility and the lattice temperature. Optimized BOI and SOI devices are selected for CMOS inverter and SRAM cell simulation. For inverters, a 5 GHz signal is applied to examine the inverter transient response. For SRAM cells, the circuits powered with a 0.6 V voltage are simulated and static noise margins (SNMs) are extracted. Transient response is also simulated to test the functionality of the SRAM. The write-0-operation time and the write-1-operation time are compared.

Subthreshold Swing (SS), Drain Induced Barrier Lowering (DIBL) are summarized in Table I for both SOI and BOI FinFETs. The buried insulator and the fin structure improve SCEs. The threshold voltage for n-Type BOI and SOI FinFET are around 0.25 V, whereas the P-type ones are around -0.26 V. The output characteristics of SOI and BOI devices are shown in Fig. 2. The BOI FinFET on-state current is slightly greater than the SOI one, but its parasitic capacitance is also larger than the SOI structure [1]. Higher current and capacitance are due to the source/drain region extension and additional junctions formed at the substrate. Simulation results shows SHE degrades on-state current of SOI FinFET but has less impact on BOI device for gate bias greater than 0.6 V [1]. However, for low voltage applications, SHE has minimal influence on both devices [4]. The transient simulation results in Fig. 3 demonstrate high speed operation capabilities of these devices with a 5 GHz signal applied. For FinFET based SRAM cell simulation, the hold butterfly which is least sensitive to noise fluctuations and the read operation which is most sensitive are extracted. The hold SNMs are 211 mV and 209 mV, whereas the read SNMs are 120 mV and 118 mV, for BOI and SOI based SRAM respectively. SOI based Cell write-1-operation and write-0-operation time are 14% and 52% faster than the BOI based one since SOI has a smaller parasitic capacitance. Extensive simulations show that with low operating voltage, BOI and SOI based digital circuits show rather similar characteristics. Also, SHE does not degrade circuit performance during low power operation.

In summary, we have compared SOI and BOI FinFET device characteristics and the performance of digital circuits designed with those devices. For low voltage supply, SHE is modest in both devices and during digital circuit operations. SOI FinFET CMOS inverter and SRAM cell characteristics are very similar to BOI ones. Considering the lesser fabrication complexity, SOI FinFET thus would be more preferable than BOI FinFET for the design of low voltage digital circuits. The authors would like to thank Synopsys, Inc., for providing the Sentaurus TCAD tool set for device simulation.

References

[1] X. Xu et al., IEEE TED, vol. 55, No. 11, pp. 3246, 2008

[2] Sentaurus TCAD Manual, Synopsys, 2010

[3] P. Feng and P. K. Ghosh, IEEE EDS New York Conf, 2010

[4] C. Fiegna et al., IEEE TED, vol.55, No. 1, pp. 233, 2008

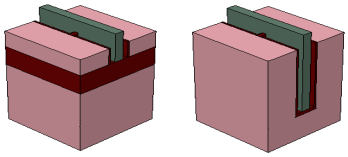

Figure 1. 3-D schematic diagram of SOI FinFET and BOI FinFET

TABLE I
DEVICE SHORT CHANNEL EFFECTS

Device	V_{th} (V)	Workfunction (eV)	DIBL (mV/V)	SS (mV)
n-type BOI	0.247	4.45	87	79.5
p-type BOI	0.263	4.45	75	-74.4
n-type SOI	0.248	4.8	68	74.7
p-type SOI	0.266	4.8	80	-75.4

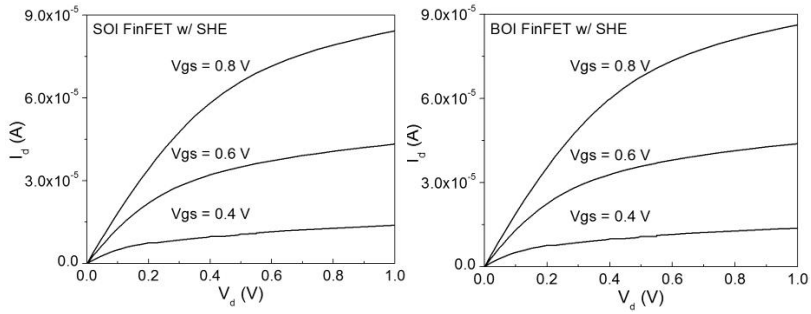

Figure 2. Output characteristics with SHE of SOI and BOI

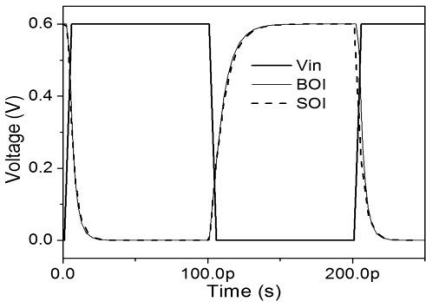

Figure 3. Transient response of CMOS inverter with a 5 GHz signal

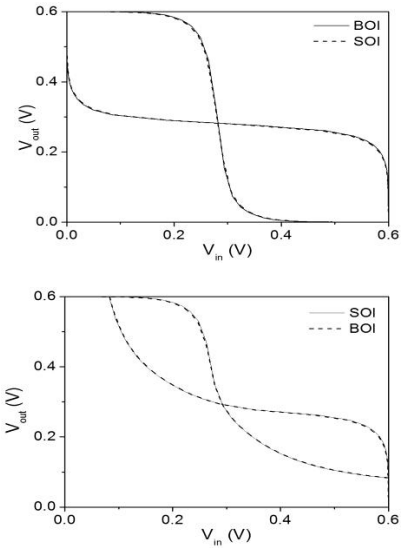

Figure 4. Hold and read butterfly characteristics for SRAM

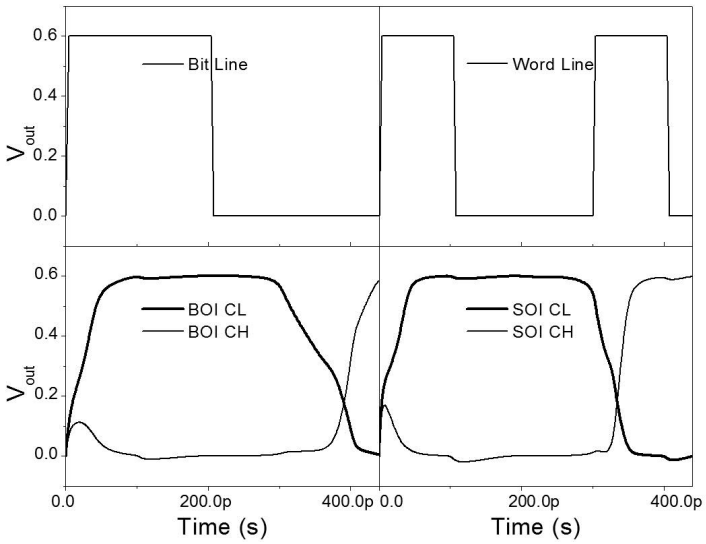

Figure 5. Transient analysis of SRAM with a 3.3 GHz word line signal